Subject: Design of electronic Circuits(E1303)

Final-Term exam - Time: 3 Hour

Semester: Sep. 2014 / Jan. 2015 - Data:5/1/2015



Electrical Eng. Dept.

Faculty of Engineering
Benha University

Answer all the following questions:

- 1. Design a BJT differential amplifier to amplify a differential input signal of 5 mV and provide a differential output signal of 0.8 V. The differential input resistance must be at least 80 K Ω . The BJTs available are specified to have $\beta = 150$. Give the circuit configuration and specify the values of all its components.
- 2. The 4-stages direct coupled op-amp circuit shown in Fig.1 is operating at room temperature. Assuming all transistors have $\beta = 200$
 - a) Perform an approximate dc analysis to calculate the current and voltage everywhere in the circuit (assuming $|V_{BE}|$ =0.7v, neglect the Early effect). Note that Q_6 has four times the area of each of Q_9 and Q_3 .
 - b) Compute the differential input resistant.
 - c) Compute the overall voltage gain of the multistage amplifier.
 - d) What is the input offset voltage if R₁ changed by 2%
- **3.** For the BJT amplifier shown in fig. 2, find the input Resistance (R_{in}) and the frequency response for the following component values:

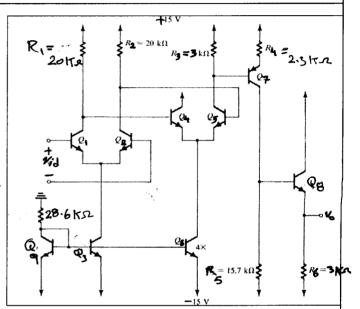
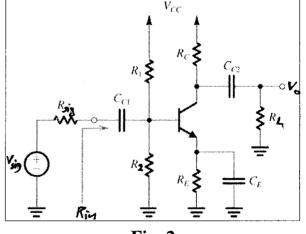
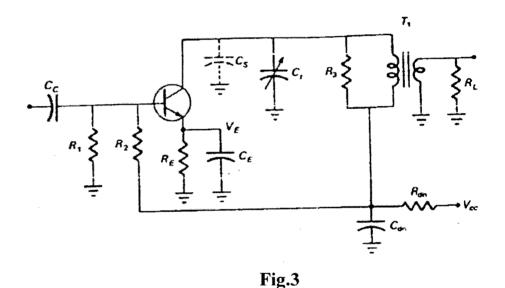


Fig. 1



- 4. Consider the complementary BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat} . For $\pm 10V$ power supplies and a 100Ω load resistance,
 - a) What is the maximum sine wave output power available?
 - b) What is the power-conversion efficiency?
 - c) Show how to reduce the zero-crossing distortion in class B power amplifier?
- 5. Design an RF amplifier shown in figure (3) for P_o (max) = 9 mW into R_L = 100 Ω at $w_o = 10^7$ rad/s and bandwidth of 10^6 rad/s. T_I consists of $X_{LI} = 100$ Ω with $Q_u = 100$ at w_o and k = 1. The transistor has $V_{be} = 0.7$, $\beta = 100$, $C_{bc} = 3$ pF, and $C_{be} = 27$ pF. For $V_{CC} = 10v$ determine:
 - a) R_1 , R_2 , and R_E .
 - b) C_t and Turns ratio of T_1 , given the bandwidth requirement.
 - c) Amplifier ac input resistance, R_{in} , and parallel capacitive reactance, X_{in} .



BEST WISHES

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Design a BJT differential amplifier to amplify a differential input signal of 5 mV and provide a differential output signal of 0.8 V. The differential input resistance must be at least 80 K Ω . The BJTs available are specified to have β = 150. Give the circuit configuration and specify the values of all its components.

Solution

Given
$$JE = IMA$$
 $Ve = \frac{VT}{JE} = \frac{25MV}{IMA} = 25\Omega$

$$I = I = 2IE = 2 \text{ mA}$$

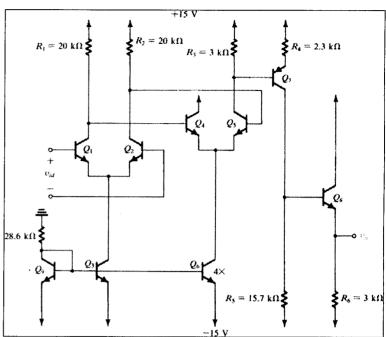
$$Av = \frac{v_0}{v_{id}} = \frac{0.8}{5m} = \frac{2Rc}{2(e+RE)} = \frac{Rc}{7e+RE}$$

I

Q2:

The 4-stages direct coupled op-amp circuit shown in Fig.1 is operating at room temperature. Assuming all transistors have $\beta = 200$

- a) Perform an approximate dc analysis to calculate the current and voltage everywhere in the circuit (assuming $|V_{BE}|=0.7v$, neglect the Early effect). Note that Q_6 has four times the area of each of Q_9 and Q_3 .
- b) Compute the differential input resistant.
- c) Compute the overall voltage gain of the multistage amplifier.
- d) What is the input offset voltage if R_1 changed by 2%

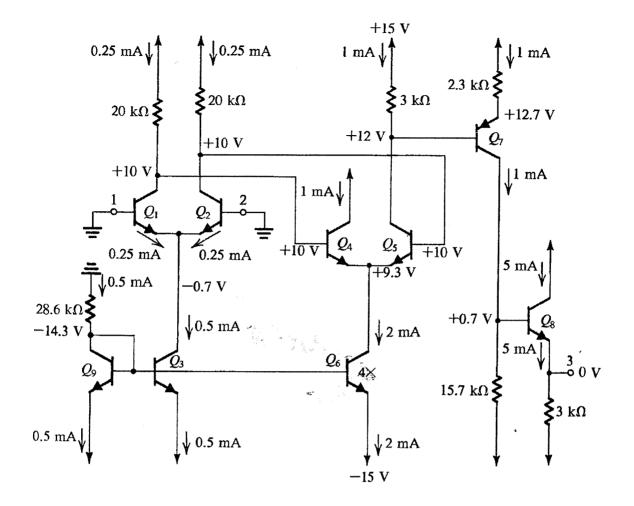


Solution:

(a) The values of all dc currents and voltages are indicated on the circuit diagram. These values were calculated by ignoring the base current of every transistor-that is, by assuming β to be very high. The analysis starts by determining the current through the diode-connected transistor Q_9 to be 0.5 mA. Then we see that transistor Q_3 conducts 0.5 mA and transistor Q_6 conducts 2mA. The current-source transistor Q_3 feeds the differential pair (Q_1, Q_2) with 0.5 mA. Thus each of Q_1 and Q_2 will be biased at 0.25 mA. The collectors of Q_1 and Q_2 will be at $[+15 - 0.25 \times 20] = +10 \text{ V}$.

Proceeding to the second differential stage formed by Q_4 and Q_5 , we find the voltage at their emitters to be [+10 - 0.7] = 9.3 V. This differential pair is biased by the current-source transistor Q_6 , which supplies a current of 2 mA; thus Q_4 and Q_5 will each be biased at 1 mA. We can now calculate the voltage at the collector of Q_5 as $[+15 - 1 \times 3] = +12$ V. This will cause the voltage at the emitter of the pnp transistor Q_7 to be +12. 7 V, and the emitter current of Q_7 will be (+15 - 12.7)/2.3 = 1 mA. The collector current of Q_7 , 1 mA, causes the voltage at the collector to be $[-15 + 1 \times 15.7] = +0.7$ V. The emitter of Q_8 will be 0.7 V below the base; thus output terminal 3 will be at 0 V.

Finally, the emitter current of Q8 can be calculated to be [0 - (-15)]/3 = 5 mA.



(b) The input differential resistance R_{id} is given by:

$$Rid = r_{\pi 1} + r_{\pi 2}$$

Since Q_1 and Q_2 are each operating at an emitter current of 0.25 mA, it follows that

$$r_{e1} = r_{e2} = 25/0.25 = 100\Omega$$

for $\beta = 200$; then

$$r_{\pi 1} = r_{\pi 2} = 201 \times 100 = 20.1 \text{ k}\Omega$$

Thus

$$R_{id} = 40.2 k\Omega$$

(c)To evaluate the gain of the first stage we first find the input resistance of the second stage, R_{i2} ,

$$R_{i2} = r_{\pi 4} + r_{\pi 5}$$

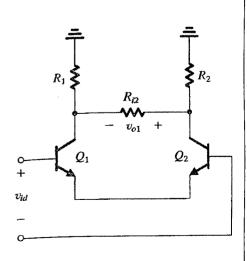
 Q_4 and Q_5 are each operating at an emitter current of 1mA; thus

$$r_{e4} = r_{e5} = 25 \Omega$$

 $r_{\pi 4} = r_{\pi 5} = 201 \text{ x} 25 = 5.025 \text{ k}\Omega$

Thus

$$R_{i2} = 10.05 \text{ k}\Omega.$$

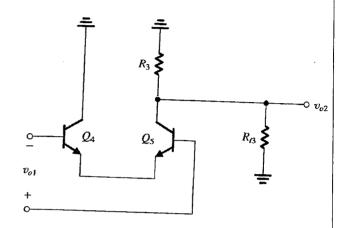


This resistance appears between the collectors of Ql and Q2, as shown in - Fig. Thus the gain of the first stage will be

A1
$$\equiv \frac{v_{o1}}{v_{id}} \cong \frac{\text{Total resistance in collector circuit}}{\text{Total resistance in emitter circuit}} = \frac{R_{i2} \parallel (R_1 + R_2)}{r_{e1} + r_{e2}}$$

$$= \frac{10.05k \parallel 40k}{200} = \frac{8031.97}{200} = 40.16 \text{ V/V}$$

Figure 2 shows an equivalent circuit for calculating the gain of the second stage. As indicated, the input voltage to the second stage is the input voltage of the first stage, v_{ol} . Also shown is the resistance R_{i3} which is the input resistance of the third stage formed by Q_7 . The value of R_{i3} can be found by multiplying the total resistance in the emitter of Q_7 by $(\beta+1)$:



$$R_{i3} = (\beta + 1)(R4 + re7)$$

Since Q₇ is operating at an emitter current of 1 mA,

$$r_{e7} = 25/1 = 25\Omega$$

$$R_{i3} = 201 \text{ x } (2.3k+25) = 467.325 \text{ k}\Omega$$

We can now find the gain A2 of the second stage as the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit:

$$A2 = \frac{v_{o2}}{v_{o1}} = -\frac{(R_3 \parallel R_{i3})}{r_{e4} + r_{e5}}$$
$$= -\frac{(3k \parallel 467.325k)}{50} = \frac{2980.86}{50} = -59.6 \text{ V/}_V$$

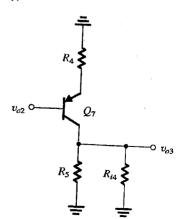
To obtain the gain of the third stage we refer to the equivalent circuit shown in Fig., where R_{i4} is the input resistance of the output stage formed by Q8. Using reflection resistance-reflection rule, we calculate the value of R_{i4} as

$$R_{i4} = (\beta + 1)(r_{e8} + R_6)$$

where

$$r_{e8} = 25/5 = 5\Omega$$

$$R_{i4} = 201(5 + 3000) = 604.005 \text{ k}\Omega$$



The gain of the third stage is given by

$$A3 = \frac{v_{o3}}{v_{o2}} = -\frac{(R_5 \parallel R_{i4})}{r_{e7} + R_4} = -\frac{(15.7k \parallel 604.005k)}{25 + 2.3k}$$
$$= -\frac{15.302k}{2.325k} = -6.58 \text{ V/V}$$

Finally, to obtain the gain A4 of the output stage we refer to the equivalent circuit in Fig. and write

$$A4 \equiv \frac{v_o}{v_{o3}} = \frac{R_6}{R_6 + r_{e8}} = \frac{3000}{3000 + 5} = 0.998 \approx 1$$

The overall voltage gain of the amplifier can then be obtained as follows:

$$\frac{v_o}{v_{id}} = A1A2A3A4 = 40.16 \times -59.6 \times -6.58 \times 1 = 15749.5$$

(d) The input offset voltage if R₁ changed by 2%

The input offset voltage V_{OS}

$$|V_{OS}| = V_T \left(\frac{\Delta R_c}{R_c}\right) = V_T \left(\frac{\Delta R_1}{R_1}\right) = 25m \times 0.02 = 0.5mV$$

Q3:

For the BJT amplifier shown in fig. 2, find the input Resistance (R_{in}) and the frequency response for the following component values:

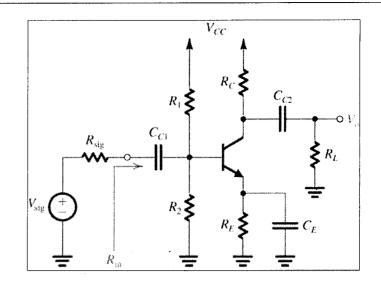
 $R_1=10k\Omega$; $R_2=10k\Omega$; $R_C=4.3k\Omega$; $R_E=6.8k\Omega$;

 R_L =1 $k\Omega$; R_{sig} =500 Ω ; Vcc=15V

 C_{C1} =0.47uF; C_{C2} =0.68uF; C_{E} =0.22uF;

 $C_{\mu} = 1 pF; C_{\pi} = 1 nF. \beta = 100$

Solution



DC Analysis

- ALL Capacitor are o.c

RB= PTh= R1 11 R2 = 10K/110K=5KR.

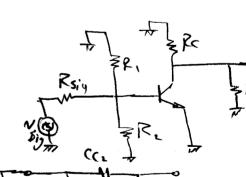
200 P (31

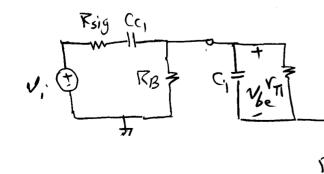
$$I_E = \frac{17h - 18E}{RE + RB} = \frac{7.5 - 0.7}{6.8K + \frac{5K}{101}} = 0.993MA$$

$$q_{y} = \frac{Tc}{\sqrt{7}} = \frac{0.98m}{25mV} = 39.2 \text{ MAIV}$$

 $\sqrt{1} = \frac{B}{\alpha W} = \frac{100}{39.2 \text{ m}} = 2.55 \text{ K.s.}$ $\sqrt{0} = W = 3.0$

Ac Analysis





For mid-band gain Avo There is no effect of capacitoons cc' = ccs = c = 2.c = c! = co = 0.c 13xy To RBF 1/2 FVTT Dynu6e FRC FRLN. Kin= RB11YT = 5K 112.55 K = 1.69 KD 1 1/2 = am RL ; RL = Rc 11 RL RL = RC11RL = 4.3K 1/1K2 = 811.3252 1 /ce | = 39.2 × 10-3 × 811.32 = 31.8 VIV Ci = CT+CMi ; CMi = CM(1+1 VC8 1) CM: = 1 pf (1+31-8) = 32-8 pf CM0 = CX(1+ / Vce)= CM = 1 P\$ = Co -To find codaff Frequency = 1.5=5.0 @ C.5=0.0 -for low frequency = Ci = Co = o.c effect of CC, put CC2 = CE = S.C Rcc, = Rsig + RB 11VT = 500+ 1.69K = 2.19 Kr. Felile = 21 (Cc, Rc,) = 211 (0.47 *106 *2.19 x103) = 154.6 HZ effect of Ccz PW C(1=6=2-0 Rcc2 = Rc+ FL = 4.3K + 1K = 5.3 K.s.

Felz = 2T (CC2 Recz) effect of CE 211 x 0.68 x 166 x 5.3 x 103 = 44.2 HZ out ca = cc 2 = 5.0 RE = RE 11 PSiy 11 RB11/7 = 6.8KII[50011 1.69K] RSig IIRBINT RET CET = 6.8 K 11 385.85 = 6.8K 11 3.82 \(\sigma \) 3.82 \(\sigma \). fcL3 | = 189.4 | THZ

L=fcL1+fcL2+fcL3=1801-6 KHZ

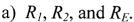
- for high frequency Response = CC1 = CC2 = CE = 5.0 effect of Ci Rsig RBTC; FVTT TCO RCS Put (= 0.0 Rc; = 12sig 11 R13 /1/11 = 500 // 1.69K = 385.851 Fenile = 1 2TT (Ci Rei) Ci = CT + (Mi = 1NF+32.8 pf = 1.0328 NF Fchil = - 399.4 KHZ effect of co put ci=oc RCo = RC || FL = RL = 811.32-1 Adrel Co = 2T (Co RCo) = 2T * 1 * 10-12 * 811.32 = 196.17 MHZ fn = fch, + fch2 = 196.569 MAZ

(8)

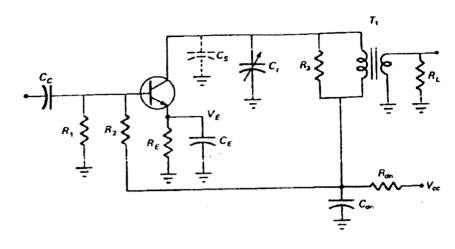
Q 4: Consider the complementary BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat} . For $\pm 10V$ power supplies and a 100 Ω load resistance, a) What is the maximum sine wave output power available? b) What is the power-conversion efficiency? c) Show how to reduce the zero-crossing distortion in class B power amplifier? Solution a) The average Load power PL = 1/2 Vo where To is The Peak amplitude of OIP sine work. - The maximum sine wave oip power occurs when To = Vcc Then PL/max = \frac{1}{2} \frac{\frac{1}{7}L} $= \frac{1}{2} \frac{(10)^2}{100} = 0.5 \, \text{W}$ (b) The power conversion efficiency 7 = Th where Ps is The Total Supply Rower Ps = Ps+ + Ps-: The average power drawn from each of The Two Power Supplies will be The Same - Then $P_{S+} = P_{S-} = \frac{1}{\pi} \frac{V_o}{RL} Vcc = \frac{1}{\pi} \frac{(1_o)}{1_{oo}} \chi_{1o} = 0.318 \,\omega$ ·· Ps = 2 *0.318 = 0.637 ~ .. The power Conversion officiency of is 2 = The x loo = 0.5 x 100 = 78.5% (c) - To reduce The Zero-crossing distortion inclass B Power Amp. by using a high-gain op-Amq. and overall negative feedback as shown The to. IN dead band is reduced to to. 7/A. volt. where As is The Occasion of op-Amt. Using bias voltage VBB applied between The busing Quandap giving rise To abias current Ice. Thus for small 1, buth Transistors Conduct and Crossover distortion is almost comptely vi eliminated as shown in Fig. (class AB off stage)

Q5:

Design an RF amplifier for P_o $(max) = 9 \text{ mW into } R_L = 100 \Omega$ at $w_0 = 10^7$ rad/s and bandwidth of 10^6 rad/s. T_I consists of X_{IJ} = 100Ω with $Q_u = 100$ at w_o and k= 1. The transistor has $V_{be} = 0.7$, β = 100, C_{bc} = 3 pF, and C_{be} = 27 pF. For V_{CC}=10v determine:



b) C_t and Turns ratio of T_1 , given the bandwidth requirement.



I2=11 [B] R.

I,=10 IB BR

c) Amplifier ac input resistance, R_{in} , and parallel capacitive reactance, X_{in} .

Solution

DC Design

Let
$$z = 5000$$
 $T_c = \frac{290}{0.9 \text{ ycc}}$
 $= \frac{2}{3} \times \frac{9}{3} \times \frac{9}{3} = \frac{9}{3} \times \frac{9}{3} \times \frac{9}{3} = \frac{9}{3} \times \frac{9}{3}$

$$T_{B} = \frac{T_{C}}{B} = \frac{2m}{100} = 0.02 \text{ mA}$$

$$T_{E} = T_{B} + T_{C} = 2m + 0.02 \text{ m} = 2.02 \text{ mA}$$

$$\text{Let } V_{E} = 0.1 \text{ VCC} = 0.1 \text{ k lo} = 1.7$$

$$R_{E} = \frac{V_{E}}{I_{E}} = \frac{1}{2.02m} = 4.95 \text{ Sc}$$

for hard potential divider let I, = 10 Is; Then Iz = 11 IB : VB = VBE + VE = 0.7 +1 = 1.7 V $R_{1} = \frac{\sqrt{13}}{7} = \frac{\sqrt{17}}{\sqrt{0.02}} = 8.5 KR$ Ri= Va - VB $= \frac{10 - 1.7}{11 \times 0.02 \, \text{m}} = 37.73 \, \text{K} \Omega$

AC Design
$$\frac{T_C}{V_0} = \frac{2mA}{25mV} = 0.08 \text{ AlV}$$

$$\frac{V_0}{V_0} = \frac{B}{V_0} = \frac{1.25 \text{ Kg}}{0.08} = 1.25 \text{ Kg}$$

(1)

:- Ct = Cy - CMo = Noopt - 3pf = 997 Pf

Ri= Ri 11P2 11Vbe= RB 11Vbe= 8-5K 1137-73K 111.25 K=1.059 1/2.

Cin = CM; 11 cbe = CM; + cbe

CM; = (1+|Avol) cbc $1Avol = 1 \frac{Va}{V6e} 1 = {}^{\infty}_{M} R_{2} = 0.08 * 1 KR = 80 VIV$ CMi = (1+80) * 3Pf = 243 Pf Cin = CMi + Cbe = 243 Pf + 27 Pf = 270 Pf $Xcin = \frac{1}{10^{7} * 270 * 15^{12}} = 370 Sc.$