Benha University	**Time: 3hour**
Benha Faculty of Engineering	**Forth Year 2014/2015**
Subject: Power Electronics (E462)	**Elect. Eng. Dept.**

Solve & draw as much as you can (questions in two pages)

Question (1) **[12] Points**

a- Explain in details the power and energy losses in a real semi-conductor switch?

b-Explain in details a single phase bridge inverter?

c-Define harmonic factor and total harmonic distortion?

d-Explain in details two methods of PWM?

Question (2) **[12] Points**

a- Explain in details a dc-dc chopper?

b- A dc-dc chopper class A has a resistive load of 10Ω and the input dc voltage Vs=220V. The switch voltage drop is 2V and the chopping frequency is 1 Khz, if the duty cycle is 50% **Determine (i)** the average output voltage **(ii)** the rms output voltage **(iii)** the output power ?

Question (3) **[12] Points**

a- Explain in details a single phase AC/AC voltage controller?

b- A single-phase full wave ac voltage controller has a resistive load of 10Ω and supply voltage of 120V, 60Hz. The delay angles of the two thyristors are equal to 90^o. (i) **Draw** the power circuit and its associated voltage and current waveforms. (ii) **Determine** the rms values of output voltage and current, (iii) the average value of the thyristor current?

P.T.O.

Question (4) **[12] Points**

a- Explain in details a single phase transformer tap-changer?

b- A single phase transformer tap-changer has a primary voltage of 240V, 60Hz. The secondary voltages are V_1=120V and V_2=120V. If the load resistance is 10Ω and firing angles of thyristors T1 and T2 are 98^o and $\pi+ 98^o$ respectively. **Determine (i)** the load voltage, **(ii)** the rms current of the four thyristors **(iii)** the rms current of the secondary windings?

Question (5) **[12] Points**

a- Explain in details a three phase bridge inverter?

b- Design a three-phase PWM inverter that drives a 30hp, variable speed, 3-phase, 12-pole, 460V, 60Hz induction motor. The DC supply is 300V and m_a=0.8 and m_f=15. Draw a block diagram of the system and use the following table to calculate the fundamental frequency line to line voltage and some dominant harmonics of line to line voltages.

	m_a				
h	0.2	0.4	0.6	0.8	1
1	0.122	0.245	0.367	0.490	0.612
$m_f \pm 2$	0.010	0.037	0.080	0.135	0.195
$2m_f \pm 1$	0.116	0.20	0.227	0.192	0.111
$3m_f \pm 2$	0.027	0.085	0.124	0.108	0.038

Answer

Question (1) **[12] Points**

a- Explain in details the power and energy losses in a real semi-conductor switch?

5.4 Power losses from manufacturers' data sheets

The total power dissipation P_d is the sum of the switching transition loss P_s, the on-conduction loss P_d, drive input device loss P_G, and the off-state leakage loss P_t.
The average total power loss is given by

$$P_d = f_s \int_0^{1/f_s} v(t)i(t)dt \qquad \text{(W)} \qquad (5.21)$$

where f_s is the switching frequency and $v(t)$ and $i(t)$ are the device instantaneous voltage and current over one complete cycle of period $1/f_s$. The usual technique for determining total power loss is to evaluate and sum together each of the individual average power loss components.

5.4.1 Switching transition power loss, P_s

Figure 5.7 shows typical power device voltage-current switching waveforms. Normally an exact solution is not required and an approximation based on straight line switching intervals is usually adequate.
For a resistive load, as derived in chapter 6

$$P_s = \frac{1}{6} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.22)$$

and for an inductive load, as derived in chapter 6

$$P_s = \tfrac{1}{2} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.23)$$

where τ is the period of the switching interval (both on and off), and V_s and I_m are the maximum voltage and current levels as shown in figure 5.7. Switching losses occur at both turn-on and turn-off.

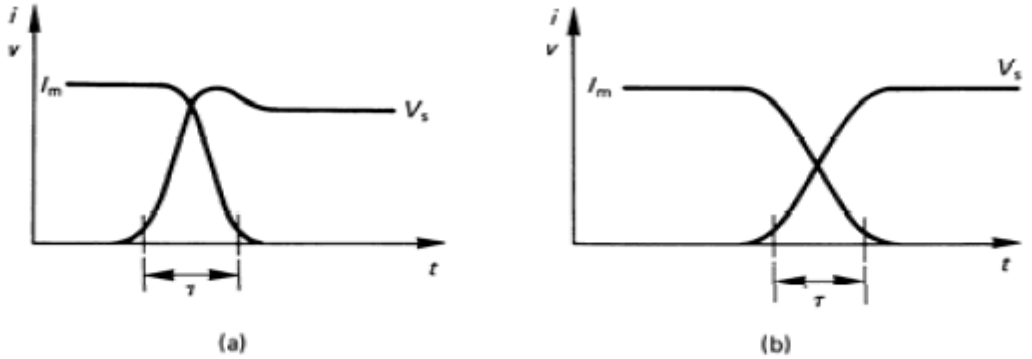


Figure 5.7. *Typical voltage and current at turn-off switching transition for: (a) an inductive load and (b) a resistive load. Current and voltage are interchanged at turn-on.*

5.4.2 *Off-state leakage power loss, P_t*

During the switched-off period, a small, exponentially temperature dependent current I_t, will flow through the switch. The loss due to this leakage current is

$$P_t = I_t V_s (1 - \delta) \qquad \text{(W)} \qquad (5.24)$$

where δ is the on-time duty cycle of the switch. Normally P_t is only a small part of the total loss so that the error in neglecting P_t is not usually significant.

5.4.3 *Conduction power loss, P_c*

The average conduction power loss under a steady-state current condition is given by

$$P_c = \delta I_{on} V_{on} \qquad \text{(W)} \qquad (5.25)$$

although equation (5.21) is valid in the general case when the integration is performed over the interval corresponding to δ.

The conduction loss for the MOSFET is usually expressed in terms of its on-state resistance (equations (3.14) and (4.12))

$$P_c = \delta\, I^2_{d(rms)} R_{ds(on)}$$
$$\simeq \delta\, I^2_{d(rms)} R_{ds(on)}(25°C)\left\{1+\frac{\alpha}{100}\right\}^{T_j-25°C} \quad \text{(W)} \tag{5.26}$$

where α is the temperature coefficient of the on-state resistance, which is positive. A linear resistance approximation of equation (5.26) is quite accurate above 25°C if α is small, such that P_c can be approximated by

$$P_c \approx \delta\, I^2_{d(rms)} R_{ds(on)}(25°C)\left\{1+\alpha\,(T_j - 25°C)\right\} \quad \text{(W)} \tag{5.27}$$

5.4.4 Drive input device power loss, P_G

A portion of the drive power is dissipated in the controlling junction or, in the case of the MOSFET, in the internal gate resistance. Usually more power is dissipated in the actual external drive circuit resistance. Drive input loss is normally small and insignificant compared with other losses, and can usually be ignored.
Two possible exceptions are:

- One notable exception is in the case of the power thyristor, where continuous gate drive is used to avoid loss of latching or when the holding current is high. The holding current can be 3% of the anode current thus the gate to cathode junction loss can be included in the total loss calculation for better accuracy. Thus, for a gate junction voltage V_{GC} the gate losses are given by

$$P_g = \delta\, I_G V_{GC} \tag{5.28}$$

  The recovery loss of the gate commutated thyristor (GCT) cathode junction can be included since it is significant because the full anode current is extracted from the gate, thus is involved in recovery of the cathode junction.
- A second exception is the MOSFET and IGBT at high switching frequencies, >50kHz, when the loss in the device, associated with providing the gate charge Q_T is given by equation (4.35):

$$P_G(R_{int}) = V_{gg} Q_T f_s \frac{R_{Gint}}{R_{Gint} + R_{Gext}} \quad \text{(W)} \tag{5.29}$$

5.5 Heat-sinking design cases

Heat-sink design is essentially the same for all power devices, but the method of determining power loss varies significantly from device type to device type. The information given in data sheets, in conjunction with the appropriate equation in table 5.2, allows the designer to calculate power semiconductor thermal rating for a variety of conditions.

5.5.1 Heat-sinking for diodes and thyristors

At low switching frequencies (<100 Hz), switching loss can be ignored. In the case of rectifying diodes or converter-grade thyristors, 50 to 60 Hz, switching loss can usually be ignored. Fast-recovery power diodes switching at less than 500Hz can also have switching losses neglected at low *VA* levels.

5.5.1i - Low-frequency switching

At a given current level I_F and on-time duty cycle δ, on-state power loss can be read directly from the manufacturers' data. Figure 5.8a illustrates loss for square-wave power pulses, while figure 5.8b illustrates loss in the case of half-wave sinusoidal current. Figure 5.8b gives energy loss per cycle, which may be converted to power when multiplied by the sinusoidal pulse frequency.

Thyristor loss due to the current waveform initial rate of rise of current, *di/dt*, can be incorporated and its contribution is added into the manufacturers' conduction loss data for a given device type.

5.5.1ii - High-frequency switching

At frequencies greater than about 100 Hz, fast-recovery diodes are normally employed and at about 500Hz, switching losses must be added to the on-state conduction loss. Diode turn-off loss is usually more significant than turn-on loss. Manufacturers provide maximum reverse recovery charge, Q_R, characteristics as shown in figure 5.9. The reverse recovery charge is a linear function of temperature and between the given junction temperatures of 25°C in figure 5.9a and 150°C in figure 5.9b, interpolation of Q_R is used.

The reverse recovery W.s/pulse, J_R, can be approximated by

$$J_R = V_R Q_R \qquad \text{(J)} \qquad (5.30)$$

where V_R is the reverse voltage applied to the diode just after turn-off. The reverse recovery average power loss is given by

$$P_s = V_R Q_R f_s \qquad \text{(W)} \qquad (5.31)$$

The total average power loss is the algebraic sum of the steady-state conduction loss and the recovery loss.

$$W = \int v_{ce}(t)\, i_c(t)\, dt \qquad \text{(J)} \qquad (6.1)$$

where the integration is performed over the switching transition period.

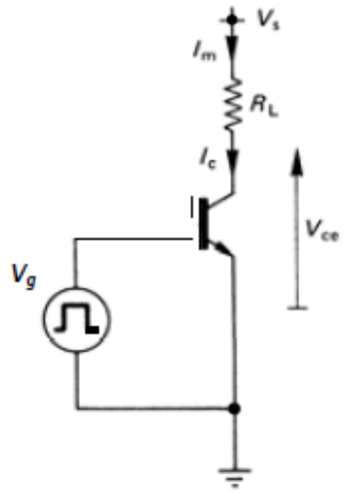


Figure 6.1. *A typical IGBT transistor switching circuit incorporating a resistive load.*

b-Explain in details a single phase bridge inverter?

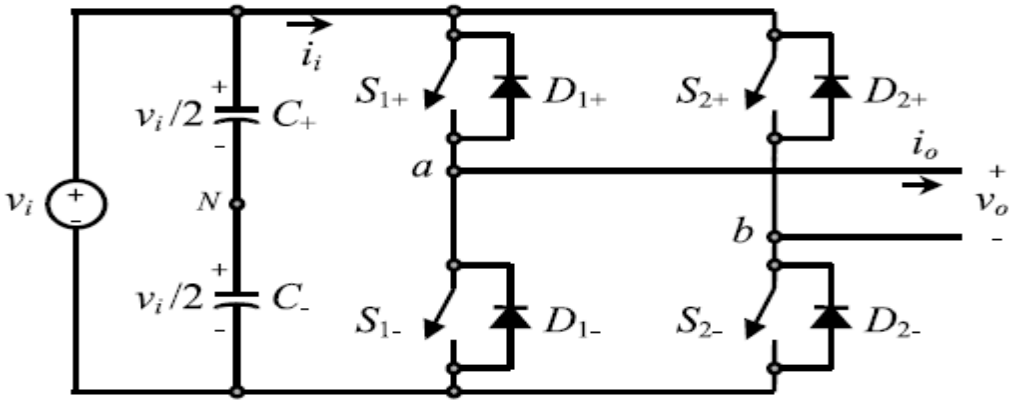


FIGURE 14.8 Single-phase full-bridge VSI.

TABLE 14.2 Switch states for a full-bridge single-phase VSI

State	State	v_a	v_b	v	Components Conducting	
$_{1+}$ and $_{2-}$ are on and $_{1-}$ and $_{2+}$ are off	1	$v/2$	$-v/2$	v	$_{1+}$ and $_{2-}$	if > 0
					$_{1+}$ and $_{2-}$	if < 0
$_{1-}$ and $_{2+}$ are on and $_{1+}$ and $_{2-}$ are off	2	$-v/2$	$v/2$	$-v$	$_{1-}$ and $_{2+}$	if > 0
					$_{1-}$ and $_{2+}$	if < 0
$_{1+}$ and $_{2+}$ are on and $_{1-}$ and $_{2-}$ are off	3	$v/2$	$v/2$	0	$_{1+}$ and $_{2+}$	if > 0
					$_{1+}$ and $_{2+}$	if < 0
$_{1-}$ and $_{2-}$ are on and $_{1+}$ and $_{2+}$ are off	4	$-v/2$	$-v/2$	0	$_{1-}$ and $_{2-}$	if > 0
					$_{1-}$ and $_{2-}$	if < 0
$_{1-}$, $_{2-}$, $_{1+}$, and $_{2+}$ are all off	5	$-v/2$	$v/2$	$-v$	$_{1-}$ and $_{2+}$	if > 0
		$v/2$	$-v/2$	v	$_{1+}$ and $_{2-}$	if < 0

c-Define harmonic factor and total harmonic distortion?

Harmonic factor HF is the measure of the individual harmonics contribution+ the rms value of the fundamental component as rms values or the ratio of the rms values of the output voltage(individual harmonics+fundamental)= $\sum V_n$ to the rms value of the fundamental component V_1

$$HF = \sqrt{\frac{V_n^2 - V_1^2}{V_1^2}} = harmonic\ f, \quad HF_n = \frac{V_n}{V_1} = harmonic\ factor\ of\ the\ nth\ harmonic$$

Total harmonic distortion factor THD is the measure of the individual harmonics (closeness in shape between a waveform and its fundamental) only contribution as rms values or the ratio of the rms values of the output voltage harmonics (individual harmonics)= $\sum V_n$ to the rms value of the fundamental component V_1

$$THF = \frac{1}{V_1}(\sum_{n=2,3,..}^{n=\alpha} V_n^2)\text{^}0.5$$

d-Explain in details two methods of PWM?

14.1.3v - Sinusoidal pulse-width modulation (pwm)

1 - Natural sampling

(a) Synchronous carrier

The output voltage waveform and method of generation for synchronous carrier, natural sampling sinusoidal pwm, suitable for the single-phase bridge of figure 14.1, are illustrated in figure 14.11. The switching points are determined by the intersection of the triangular carrier wave f_c and the reference modulation sine wave f_o. The output frequency is at the sine wave frequency f_o and the output

(b) Asynchronous carrier

When the carrier is not an interger multiple of the modulation waveform, asynchronous modulation results. Because the output frequency, f_o, is usually variable over a wide range, it is difficult to ensure $f_c = nf_o$. To achieve synchronism, the carrier frequency must vary with frequency f_o. Simpler generating systems result if a fixed carrier frequency is used, resulting in asynchronism

2 - Regular sampling

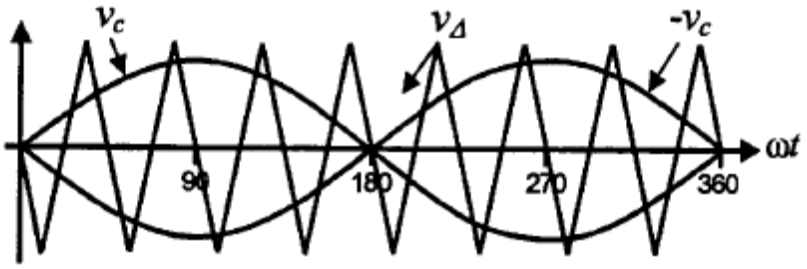
Asynchronous carrier

When a fixed carrier frequency is used, usually no attempt is made to synchronise the modulation frequency. The output waveforms do not have quarter-wave symmetry which produces subharmonics. These subharmonics are insignificant if $f_c >> f_o$, usually, $f_c > 20 f_o$.

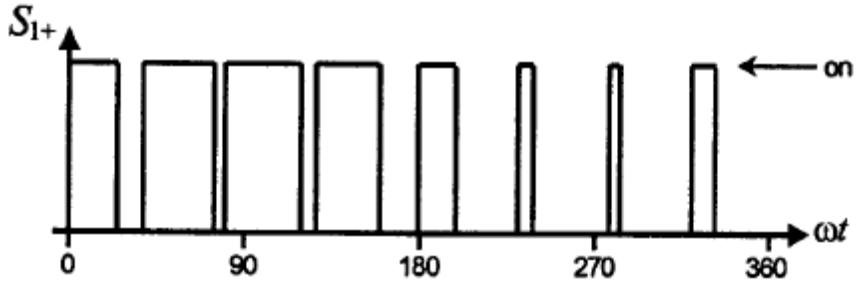
Asymmetrical modulation

Asymmetrical modulation is produced when the carrier is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency, as shown in figure 14.13b. Each side of the triangular carrier about a sampling point intersects the stepped waveform at different step levels. The resultant pulse width is asymmetrical about the sampling point, as illustrated by the lower pulse in figure 14.14 for two modulation waveform magnitudes. The pulse width is given by

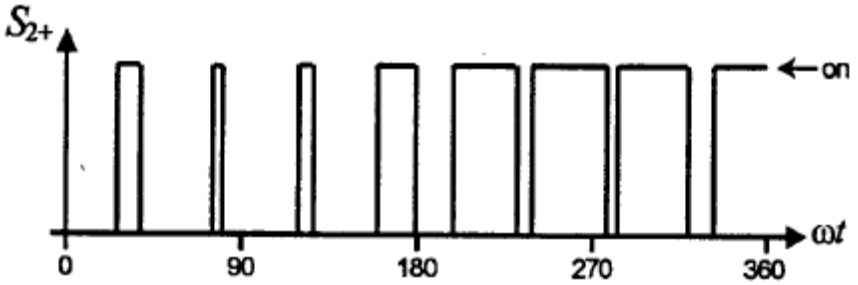
$$t_{pa} = \frac{1}{2f_c}\left(1 - \tfrac{1}{2}M\left(\sin 2\pi f_o t_1 + \sin 2\pi f_o t_2\right)\right) \qquad (14.45)$$


v_c
v_Δ
$-v_c$
90
180
270
360
ωt

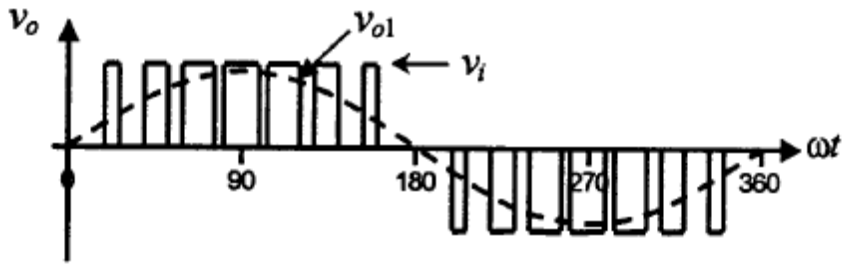
a)


S_{1+}
on
ωt
0
90
180
270
360

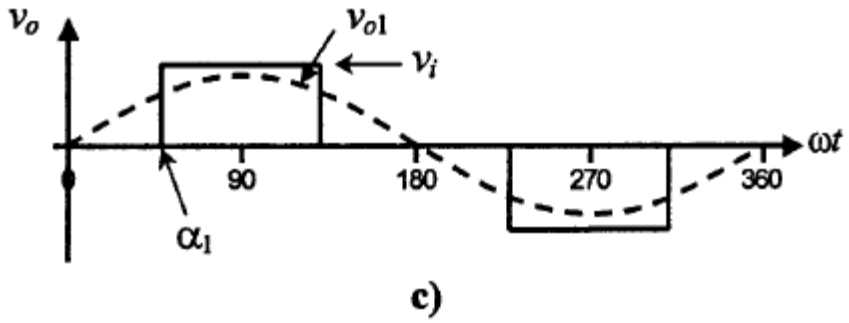
b)


S_{2+}
on
ωt
0
90
180
270
360

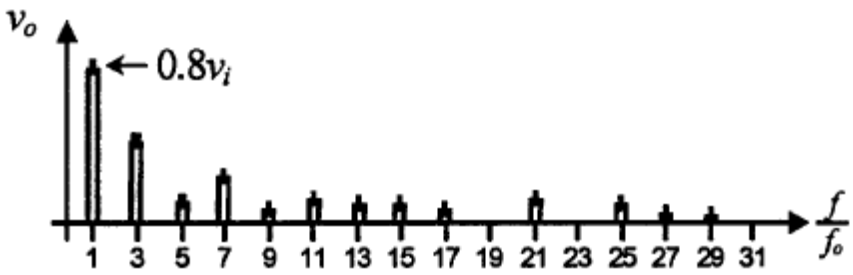
c)


v_o
v_{o1}
v_i
ωt
90
180
270
360

d)



c)



d)

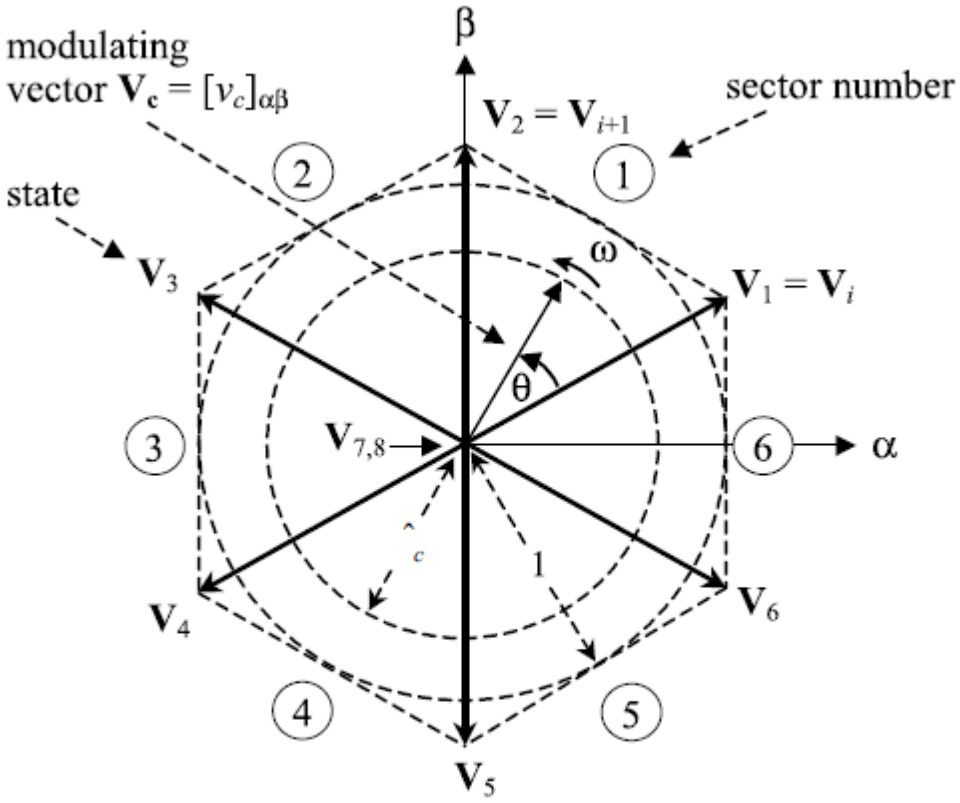


FIGURE 14.18 The space-vector representation.

Question (2) **[12] Points**

a- Explain in details a dc-dc chopper?

A step-down dc chopper with a resistive load is shown in Fig. 13.1a. It is a series connection of a dc input voltage source V_S, controllable switch S, and load resistance R. In most cases, switch S has unidirectional voltage-blocking capabilities and unidirectional current-conduction capabilities. Power electronic switches are usually implemented with power MOSFETs, IGBTs, MCTs, power BJTs, or GTOs. If an antiparallel diode is forms in a step-down chopper. The switch is being operated with a duty ratio D defined as a ratio of the switch *on* time to the sum of the *on* and *off* times. For a constant frequency operation

$$D \equiv \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} = \frac{t_{\text{on}}}{T} \tag{13.1}$$

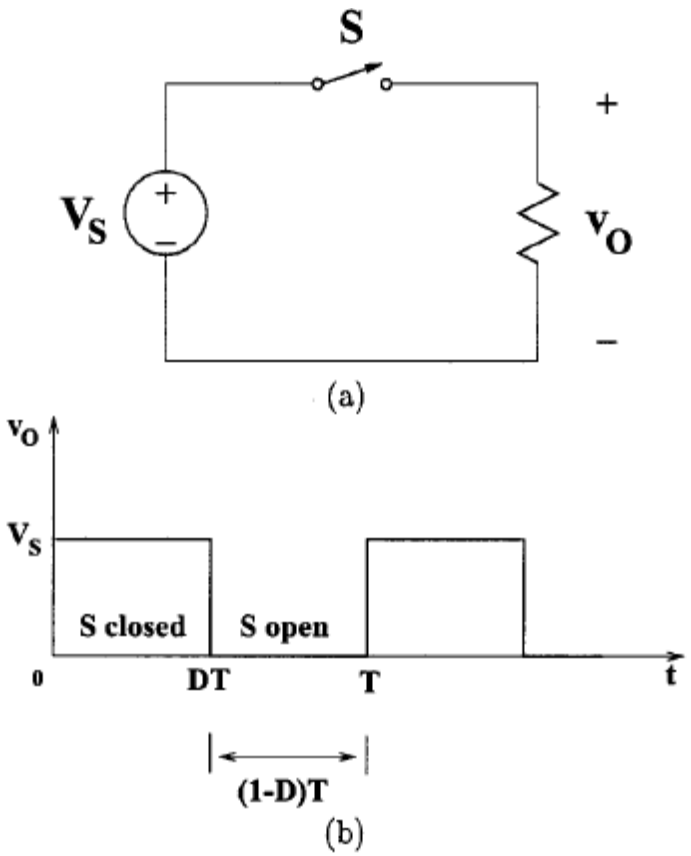


FIGURE 13.1 DC chopper with resistive load: (a) circuit diagram; (b) output voltage waveform.

where $T = 1/f$ is the period of the switching frequency f. The average value of the output voltage is

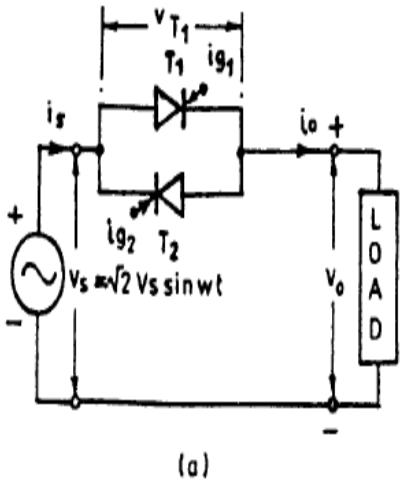
$$V_O = DV_S \qquad (13.2)$$

b-A dc-dc chopper class A has a resistive load of 10Ω and the input dc voltage Vs=220V. The switch voltage drop is 2V and the chopping frequency is 1 Khz, if the duty cycle is 50% **Determine (i)** the average output voltage **(ii)** the rms output voltage **(iii)** the output power ?

V_o=0.5*220=110V, V_{rms}=$(0.5)^{\wedge 0.5}$*220=155.6V,Po=0.5*220*220*/10=2420W

Question (3) **[12] Points**

a-Explain in details a single phase AC/AC voltage controller?



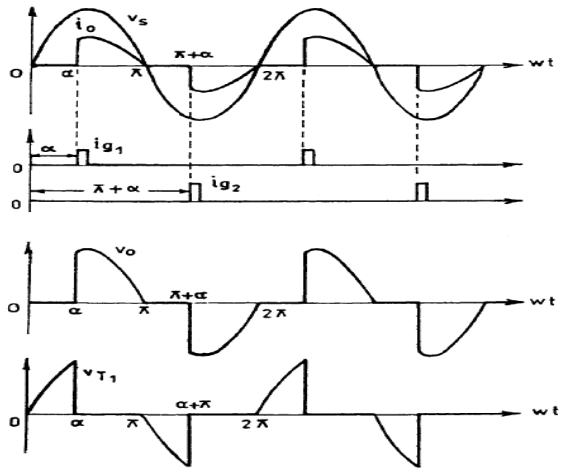


FIGURE 16.2 Waveforms for single-phase ac full-wave voltage controller with *R*-load.

b-A single-phase full wave ac voltage controller has a resistive load of 10Ω and supply voltage of 120V, 60Hz. The delay angles of the two thyristors are equal to 90^o. (i) **Draw** the power circuit and its associated voltage and current waveforms. (ii) **Determine** the rms values of output voltage and current, (iii) the average value of the thyristor current?

V_o=120[(1/pi)(pi-90+(sin2*90)/2))]^0.5=84.85V,

$I_o=V_o/R=84.85/10=8.485A, I_{th}=[(1+\cos 90)120*2^{\wedge 0.5}]/2pi*10=2.7A$

P.T.O.

Question (4) **[12] Points**

a-Explain in details a single phase transformer tap-changer?

12.4 Single-phase transformer tap-changer

Figure 12.7 shows a single-phase tap changer where the tapped ac voltage supply can be provided by a tapped transformer or autotransformer.
Thyristor T_3 (T_4) is triggered at zero voltage cross-over, then under phase control T_1 (T_2) is turned on. The output voltage for a resistive load is defined by

$$v_o = \sqrt{2}\,V_2 \sin\omega t \quad \text{(V)} \qquad \text{for } 0 \le \omega t \le \alpha \quad \text{(rad)} \tag{12.22}$$

$$v_o = \sqrt{2}\,V_1 \sin\omega t \quad \text{(V)} \qquad \text{for } \alpha \le \omega t \le \pi \quad \text{(rad)} \tag{12.23}$$

where α is the phase delay angle and $v_2 < v_1$.
For a resistive load the rms output voltage is

$$V_{rms} = \left[\frac{V_2^2}{\pi}(\alpha - \tfrac{1}{2}\sin 2\alpha) + \frac{V_1^2}{\pi}(\pi - \alpha + \tfrac{1}{2}\sin 2\alpha)\right]^{1/2} \tag{12.24}$$

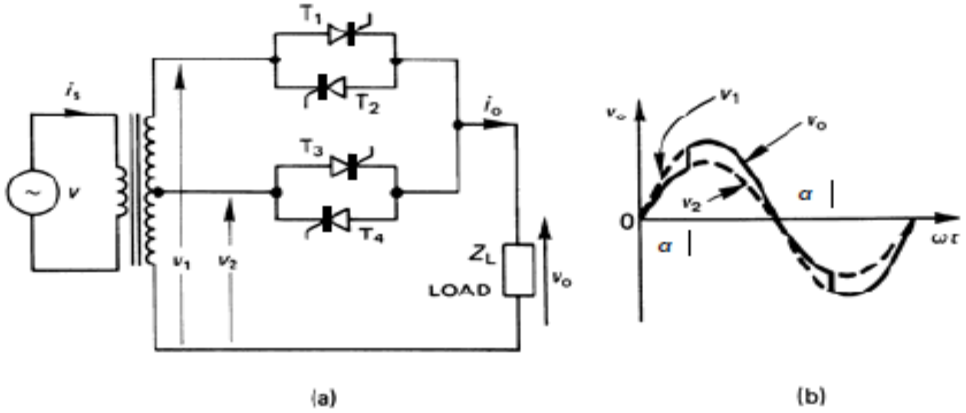


Figure 12.7. *An ac voltage regulator using a tapped transformer: (a) circuit connection and (b) output voltage waveform with a resistive load.*

Initially v_2 is impressed across the load. Turning on T_1 (T_2) reverse-biases T_3 (T_4), hence T_3 (T_4) turns off and the load voltage jumps to v_1. It is possible to vary the rms load voltage between v_2 and v_1. It is important that T_1 (T_2) and T_4 (T_3) do not conduct simultaneously, since such conduction short-circuits the transformer secondary.
With an inductive load circuit, when only T_1 and T_2 conduct, the output current is

$$i_o = \frac{\sqrt{2}\,V}{Z}\sin(\omega t - \phi) \quad \text{(A)} \tag{12.25}$$

where $Z = \sqrt{R^2 + (\omega L)^2}$ (ohms) $\qquad \phi = \tan^{-1}\omega L / R$ (rad)
It is important that T_3 and T_4 are not fired until $\alpha \ge \phi$, when the load current must have reached zero. Otherwise a transformer secondary short circuit occurs through T_1 (T_2) and T_4 (T_3).
For a resistive load, the thyristor rms currents for T_3, T_4 and T_1, T_2 respectively are

$$I_{T_{rms}} = \frac{v_2}{2R}\sqrt{\frac{1}{\pi}(2\alpha - \sin 2\alpha)}$$
$$I_{T_{rms}} = \frac{v_1}{2R}\sqrt{\frac{1}{\pi}(\sin 2\alpha - 2\alpha) + 2\pi} \qquad (12.26)$$

The thyristor voltages ratings are both v_1 - v_2, provided a thyristor is always conducting at any instant.

An extension of the basic operating principle is to use phase control on thyristors T_3 and T_4 as well as T_1 and T_2. It is also possible to use tap-changing in the primary circuit. The basic principle can also be extended from a single tap to a multi-tap transformer.

The basic operating principle of any multi-output tap changer, in order to avoid short circuits, independent of the load power factor is

- switch up in voltage when the load V and I have the same direction, delivering power
- switch down when V and I have the opposite direction, returning power.

b-A single phase transformer tap-changer has a primary voltage of 240V, 60Hz. The secondary voltages are V_1=120V and V_2=120V. If the load resistance is 10Ω and firing angles of thyristors T1 and T2 are 98^o and π+ 98^o respectively. **Determine (i)** the load voltage, **(ii)** the rms current of the four thyristors **(iii)** the rms current of the secondary windings?

$V_o=[(V_1^2/pi)(\alpha-(\sin 2\alpha)/2]+((V_1+V_2)^2/pi)(pi-\alpha+(\sin 2\alpha)/2)]^{0.5}=180V$

$I_{R1(T1,T2)}=((V_1+V_2)/(1.414R))[(1/pi)(pi-\alpha+(\sin 2\alpha)/2)]^{0.5}=10.9A$

$I_{R3(T3,T4)}=(V_1)/(1.414R))[(1/pi)(\alpha-(\sin 2\alpha)/2)]^{0.5}=6.5A$

$I_{sec.1(T1,T2)}=1.414I_{R1}=15.4A$

$I_{sec.2(T1,T2,T3,T4)}= [(1.414I_{R1})^2+(1.414I_{R3})^2]^{0.5}=17.94A$

Question (5) **[12] Points**

a- Explain in details a three phase bridge inverter?

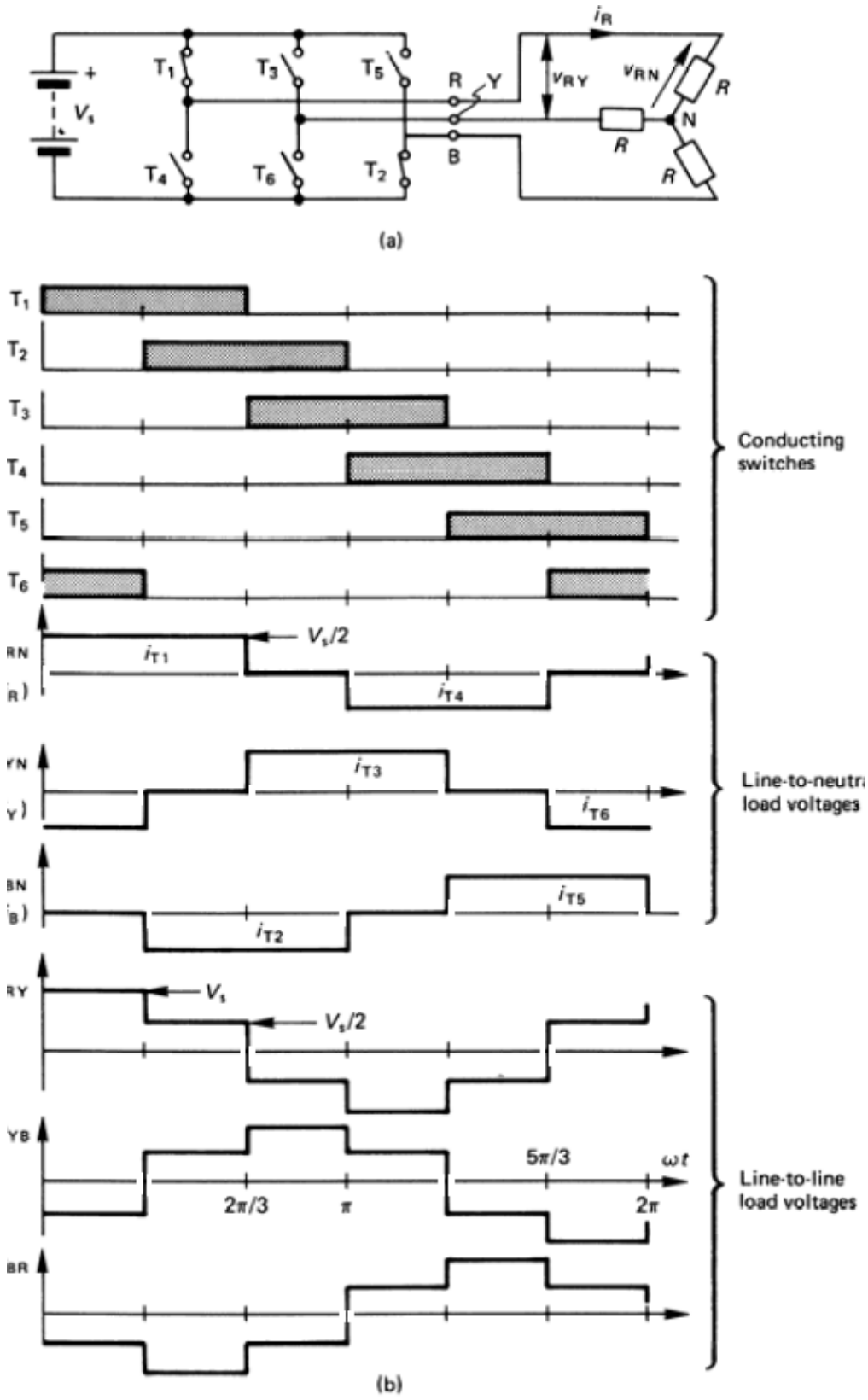


Figure 14.7. *A three-phase bridge inverter employing 120° switch conduction with a resistive star load: (a) the bridge circuit showing T_1 and T_2 conducting and (b circuit voltage and current waveforms.*

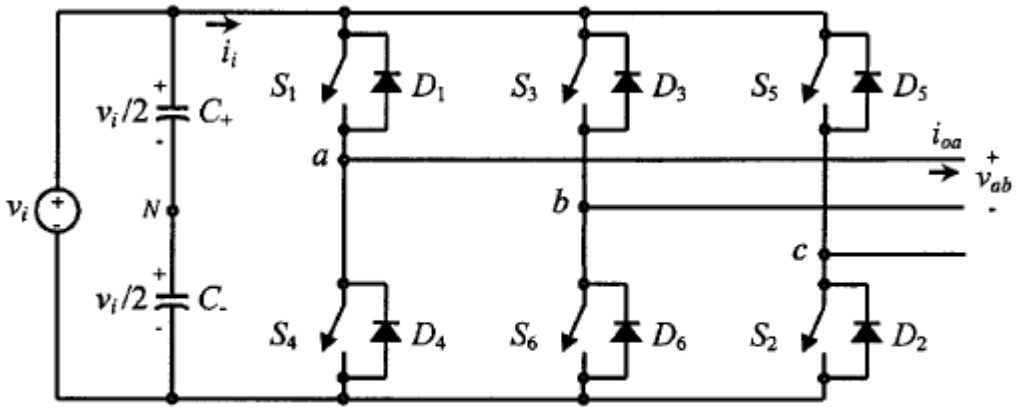
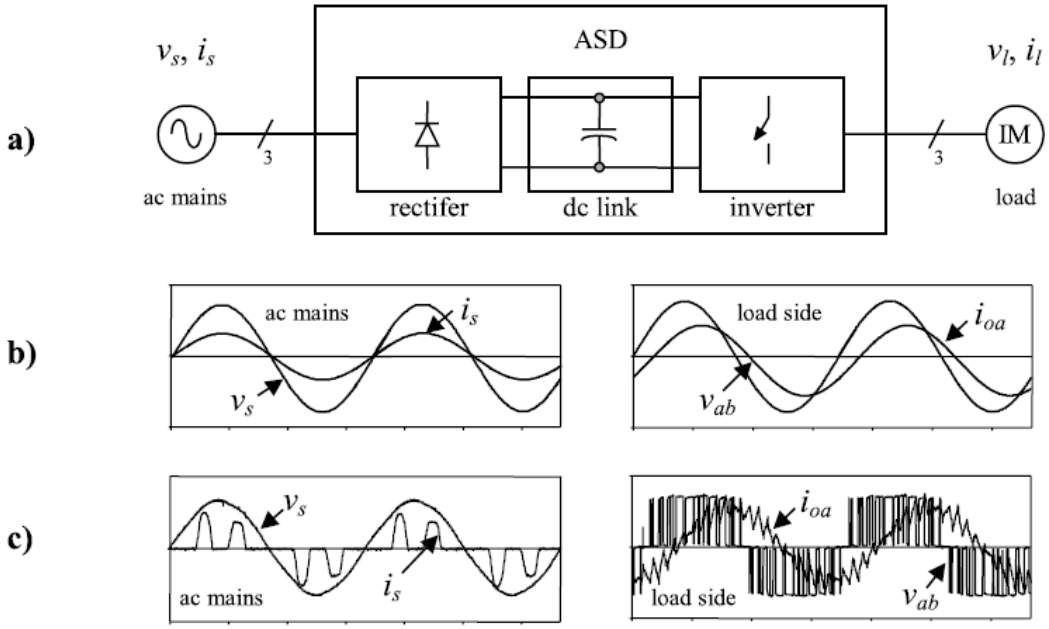


FIGURE 14.13 Three-phase VSI topology.



c- Design a three-phase PWM inverter that drives a 30hp, variable speed, 3-phase, 12-pole, 460V, 60Hz induction motor. The DC supply is 300V and m_a=0.8 and m_f=15. Draw a block diagram of the system and use the following table to calculate the fundamental frequency line to line voltage and some dominant harmonics of line to line voltages.

	m_a				
h	0.2	0.4	0.6	0.8	1
1	0.122	0.245	0.367	0.490	0.612
$m_f \pm 2$	0.010	0.037	0.080	0.135	0.195

$2m_f \pm 1$	0.116	0.20	0.227	0.192	0.111
$3m_f \pm 2$	0.027	0.085	0.124	0.108	0.038

$V_1=0.612*m_a*V_s=0.612*300*0.49=90V$

$V_{13,17}=0.612*m_a*V_s=0.612*300*0.135=32.4V$

$V_{29,31}=0.612*m_a*V_s=0.612*300*0.192=46.1V$

$V_{43,47}=0.612*m_a*V_s=0.612*300*0.108=25.9V$