Faculty of Engineering
Benha university
Electrical Eng.Dept.
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Design of Electronic Circuits(E1303)
Final-Term Exam (Corrective)
Date: 3/1/2016
Time: 3 Hours

Answer all the following questions:

1. Design a BJT differential amplifier to amplify a differential input signal of 5 mV and provide a differential output signal of 0.8 V. The differential input resistance must be at least 80 KΩ. The BJTs available are specified to have I_E=1mA and β = 150. Give the circuit configuration and specify the values of all its components.

2. The 4-stages direct coupled op-amp circuit shown in Fig.1 is operating at room temperature. Assuming all transistors have $\beta = 200$
   a) Perform an approximate dc analysis to calculate the current and voltage everywhere in the circuit (assuming $|V_{BE}|$=0.7v, neglect the Early effect). Note that Q_6 has four times the area of each of Q_9 and Q_3.
   b) Compute the differential input resistant.
   c) Compute the overall voltage gain of the multistage amplifier.
   d) What is the input offset voltage if R_1 changed by 2%

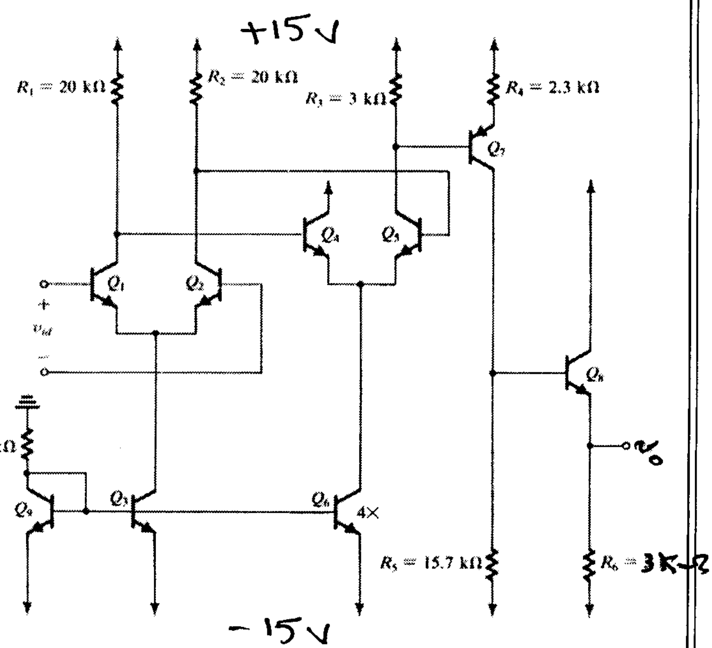


Fig. 1

3. For the BJT amplifier shown in fig. 2, find the input Resistance (R_{in}) and the frequency response for the following component values:
   R_1=10kΩ; R_2=10kΩ; R_C=4.3kΩ; R_E=6.8kΩ; R_L=1kΩ;R_{sig}=500Ω; Vcc=15V;β=100
   C_{C1}=0.47uF;C_{C2}=0.68uF; C_E=0.22uF; C_μ=1pF; C_π=1nF.

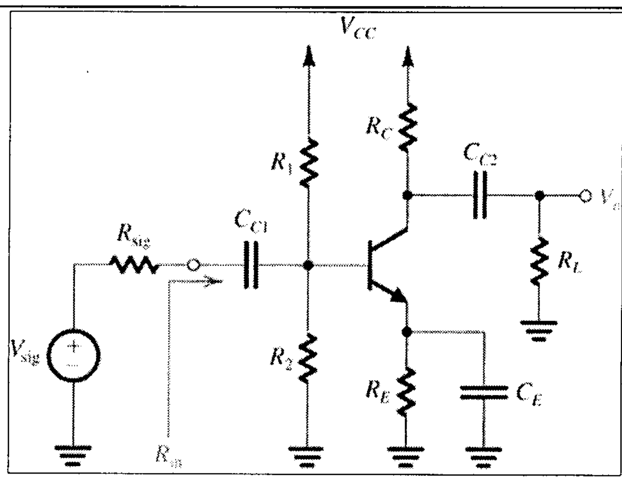


Fig. 2

4. Consider the complementary BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat}. For ±10V power supplies and a 100Ω load resistance,

   a) What is the maximum sine wave output power available?

   b) What is the power-conversion efficiency?

   c) Show how to reduce the zero-crossing distortion in class B power amplifier?

5. Design an RF amplifier shown in figure (3) for P_o (max) = 9 mW into R_L = 100 Ω at $w_o = 10^7$ rad/s and bandwidth of 10^6 rad/s. T_1 consists of X_{L1} = 100 Ω with Q_u = 100 at w_o and k = 1. The transistor has V_{be} = 0.7, β= 100, C_{bc} = 3 pF, and C_{be} = 27 pF. For V_{CC}=10v determine:

   a) R_1, R_2, and R_E.

   b) C_t and Turns ratio of T_1, given the bandwidth requirement.

   c) Amplifier ac input resistance, R_{in}, and parallel capacitive reactance, X_{in}.

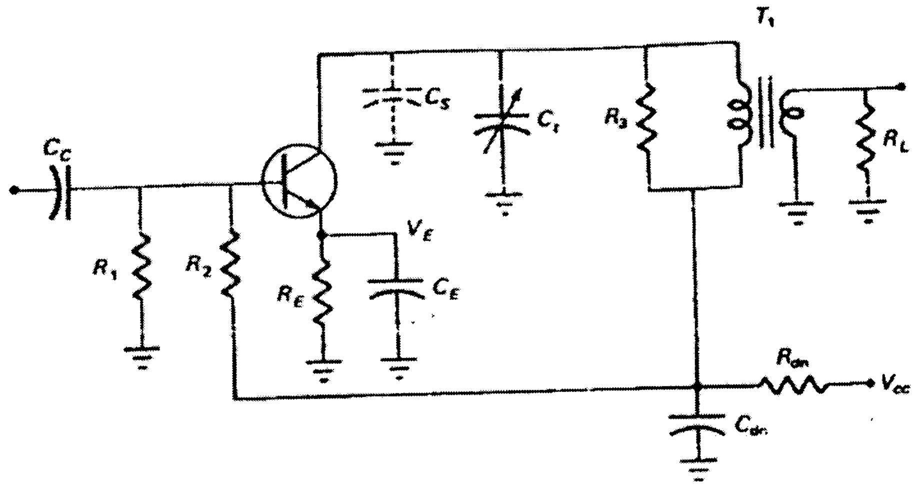


Fig.3

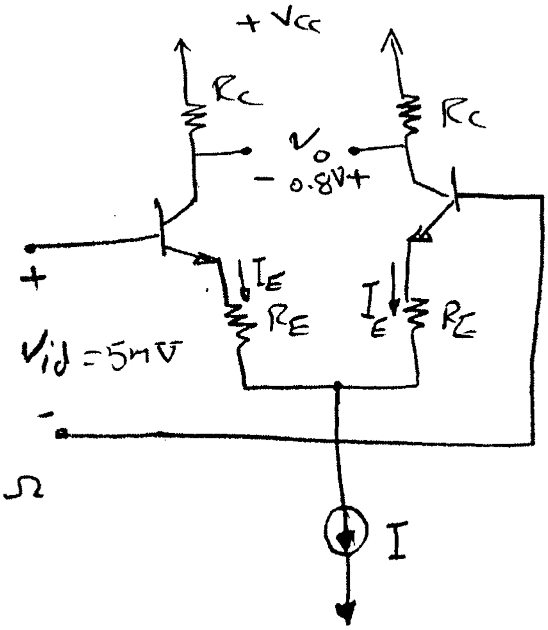
BEST WISHES

Hossam Labib

Q1:

Design a BJT differential amplifier to amplify a differential input signal of 5 mV and provide a differential output signal of 0.8 V. The differential input resistance must be at least 80 KΩ. The BJTs available are specified to have β = 150. Give the circuit configuration and specify the values of all its components.

Solution



given $I_E = 1mA$

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{1mA} = 25\,\Omega$$

$$\therefore R_{id} = 2(1+\beta)(r_e + R_E)$$

$$80K = 2(1+150)(r_e + R_E)$$

$$r_e + R_E = \frac{80K}{2 \times 151} = 264.9\,\Omega \simeq 265\,\Omega$$

$$\therefore R_E = 265 - 25 = 240\,\Omega$$

$$\because I_E = 1mA \Rightarrow I = 2I_E = 2mA$$

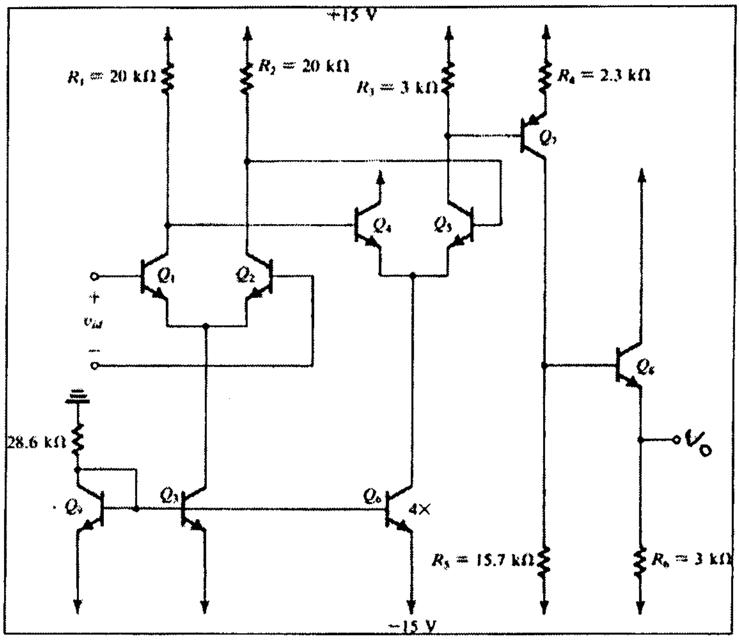
$$A_v = \frac{v_o}{v_{id}} = \frac{0.8}{5m} = \frac{2R_C}{2(r_e + R_E)} = \frac{R_C}{r_e + R_E}$$

$$\therefore 160 = \frac{R_C}{r_e + R_E}$$

$$R_C = 160(r_e + R_E) = 160 \times 265 = 42.4\,K\Omega.$$

Q2:

The 4-stages direct coupled op-amp circuit shown in Fig.1 is operating at room temperature. Assuming all transistors have $\beta = 200$



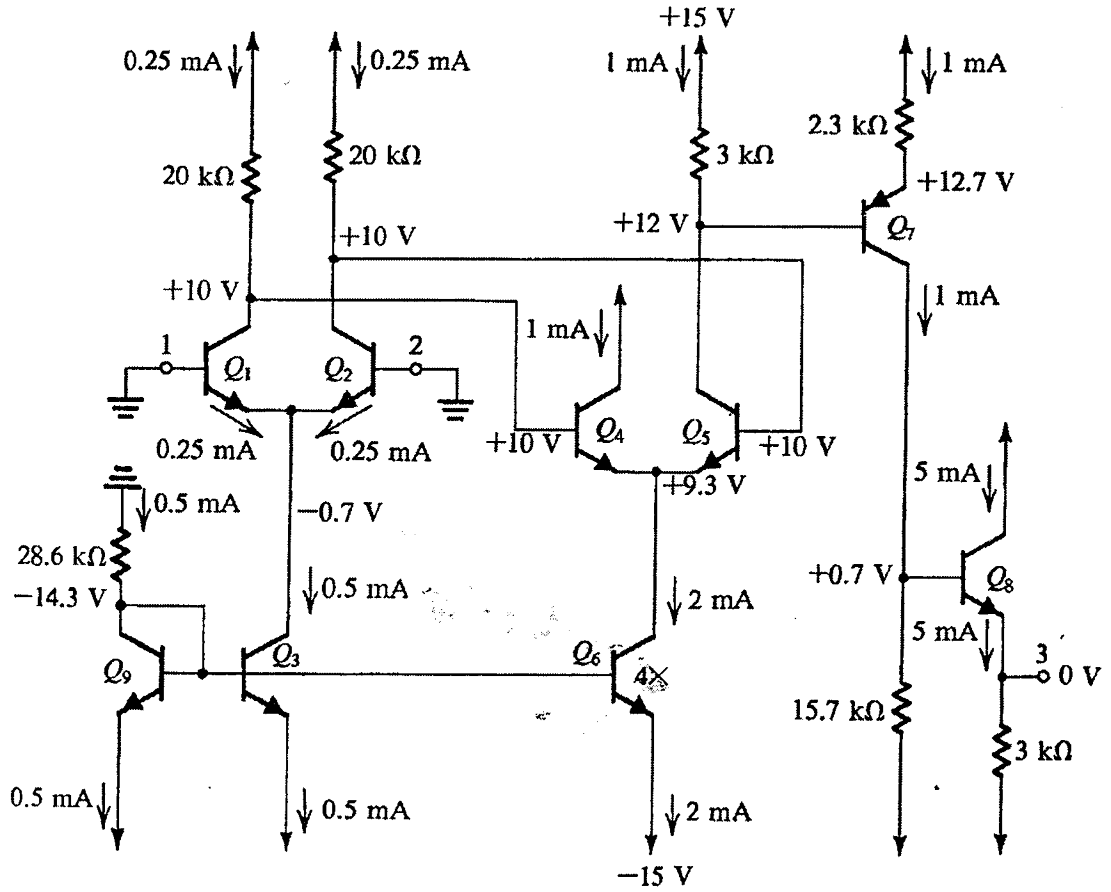
a) Perform an approximate dc analysis to calculate the current and voltage everywhere in the circuit (assuming $|V_{BE}|$=0.7v, neglect the Early effect). Note that Q_6 has four times the area of each of Q_9 and Q_3.
b) Compute the differential input resistant.
c) Compute the overall voltage gain of the multistage amplifier.
d) What is the input offset voltage if R_1 changed by 2%

Solution:

(a) The values of all dc currents and voltages are indicated on the circuit diagram. These values were calculated by ignoring the base current of every transistor-that is, by assuming β to be very high. The analysis starts by determining the current through the diode-connected transistor Q_9 to be 0.5 mA. Then we see that transistor Q_3 conducts 0.5 mA and transistor Q_6 conducts 2mA. The current-source transistor Q_3 feeds the differential pair (Q_1, Q_2) with 0.5 mA. Thus each of Q_1 and Q_2 will be biased at 0.25 mA. The collectors of Q_1 and Q_2 will be at [+15 - 0.25 x 20] =+10 V.

Proceeding to the second differential stage formed by Q_4 and Q_5, we find the voltage at their emitters to be [+10 - 0.7] = 9.3 V. This differential pair is biased by the current-source transistor Q_6, which supplies a current of 2 mA; thus Q_4 andQ_5 will each be biased at 1 mA. We can now calculate the voltage at the collector of Q_5 as [+15 - 1 x 3] = +12 V. This will cause the voltage at the emitter of the pnp transistor Q_7 to be + 12. 7 V, and the emitter current of Q_7 will be (+15 -12.7)/2.3 = 1 mA. The collector current of Q_7, 1 mA, causes the voltage at the collector to be [-15 + 1 x 15.7] = +0.7 V. The emitter of Q_8 will be 0.7 V below the base; thus output terminal 3 will be at 0 V.

Finally, the emitter current of Q8 can be calculated to be [0 - (-15)]/3 = 5 mA.



(b)The input differential resistance R_{id} is given by:

$$Rid = r_{\pi 1} + r_{\pi 2}$$

Since Q_1 and Q_2 are each operating at an emitter current of 0.25 mA, it follows that

$$r_{e1}=r_{e2}= 25/0.25=100\Omega$$

for $\beta = 200$; then

$$r_{\pi 1}= r_{\pi 2} = 201 \times 100 = 20.1\ k\Omega$$

Thus $\quad R_{id} = 40.2k\Omega$

(c)To evaluate the gain of the first stage we first find the input resistance of the second stage, R_{i2},

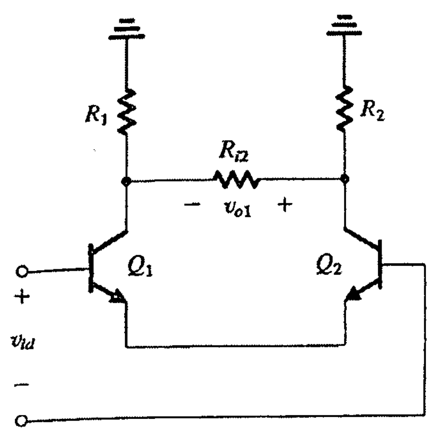
$$R_{i2} = r_{\pi 4}+ r_{\pi 5}$$

Q_4 and Q_5 are each operating at an emitter current of 1mA; thus

$$r_{e4} = r_{e5} = 25\ \Omega$$

$$r_{\pi 4}= r_{\pi 5}= 201 \times 25 = 5.025\ k\Omega$$

Thus $\quad R_{i2} = 10.05\ k\Omega.$



This resistance appears between the collectors of Ql and Q2, as shown in - Fig. Thus the gain of the first stage will be

$$A1 \equiv \frac{v_{o1}}{v_{id}} \cong \frac{\text{Total resistance in collector circuit}}{\text{Total resistance in emitter circuit}} = \frac{R_{i2} \parallel (R_1 + R_2)}{r_{e1} + r_{e2}}$$

$$= \frac{10.05k \parallel 40k}{200} = \frac{8031.97}{200} = 40.16 \ {}^{V}/_{V}$$

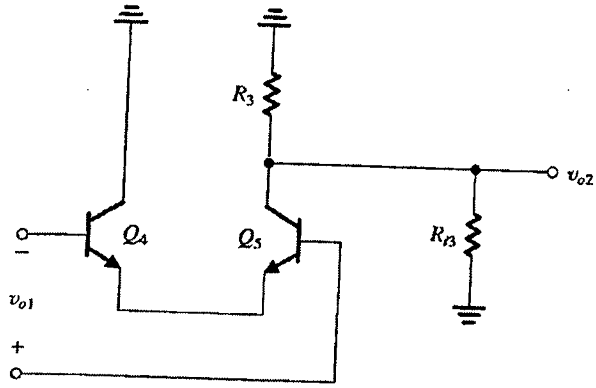


Figure 2 shows an equivalent circuit for calculating the gain of the second stage. As indicated, the input voltage to the second stage is the input voltage of the first stage, v_{o1}. Also shown is the resistance R_{i3} which is the input resistance of the third stage formed by Q_7 .The value of R_{i3} can be found by multiplying the total resistance in the emitter of Q_7 by (β+ 1):

$$R_{i3} = (\beta + 1)(R4 + re7)$$

Since Q_7 is operating at an emitter current of 1 mA,

$$r_{e7} = 25/1 = 25\Omega$$

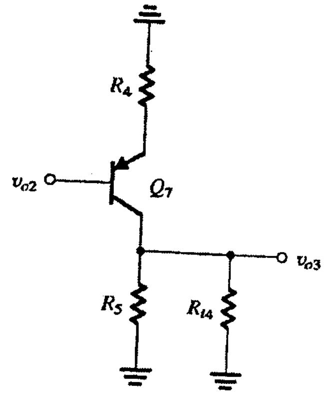
$$R_{i3} = 201 \text{ x } (2.3k+25) = 467.325 \text{ k}\Omega$$

We can now find the gain A2 of the second stage as the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit:

$$A2 = \frac{v_{o2}}{v_{o1}} = -\frac{(R_3 \parallel R_{i3})}{r_{e4} + r_{e5}}$$

$$= -\frac{(3k \parallel 467.325k)}{50} = \frac{2980.86}{50} = -59.6 \ {}^{V}/_{V}$$

To obtain the gain of the third stage we refer to the equivalent circuit shown in Fig., where R_{i4} is the input resistance of the output stage formed by Q8. Using reflection resistance-reflection rule, we calculate the value of R_{i4} as



$$R_{i4} = (\beta + 1)(r_{e8} + R_6)$$

where

$$r_{e8} = 25/5 = 5\Omega$$

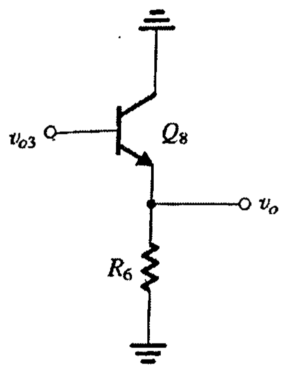
$$R_{i4} = 201(5 + 3000) = 604.005 \text{ k}\Omega$$

The gain of the third stage is given by

$$A3 \equiv \frac{v_{o3}}{v_{o2}} = -\frac{(R_5 \parallel R_{i4})}{r_{e7} + R_4} = -\frac{(15.7k \parallel 604.005k)}{25 + 2.3k}$$

$$= -\frac{15.302k}{2.325k} = -6.58\ {}^{V}/_{V}$$

Finally, to obtain the gain A4 of the output stage we refer to the equivalent circuit in Fig. and write



$$A4 \equiv \frac{v_o}{v_{o3}} = \frac{R_6}{R_6 + r_{e8}} = \frac{3000}{3000 + 5} = 0.998 \simeq 1$$

The overall voltage gain of the amplifier can then be obtained as follows:

$$\frac{v_o}{v_{id}} = A1A2A3A4 = 40.16 \times -59.6 \times -6.58 \times 1 = 15749.5$$

(d) The input offset voltage if R_1 changed by 2%

The input offset voltage V_{OS}

$$|V_{OS}| = V_T\left(\frac{\Delta R_c}{R_c}\right) = V_T\left(\frac{\Delta R_1}{R_1}\right) = 25m \times 0.02 = 0.5mV$$

Q3:

For the BJT amplifier shown in fig. 2, find the input Resistance (R_{in}) and the frequency response for the following component values:

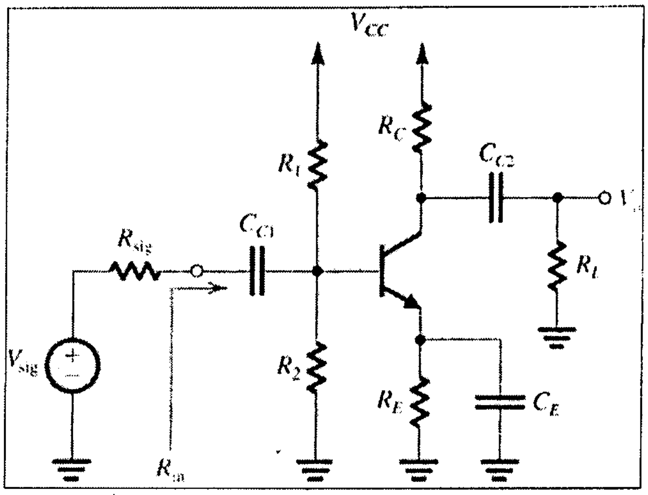
R_1=10kΩ; R_2=10kΩ; R_C=4.3kΩ; R_E=6.8kΩ;

R_L=1kΩ; R_{sig}=500Ω; Vcc=15V

C_{C1}=0.47uF; C_{C2}=0.68uF; C_E=0.22uF;

C_μ=1pF; C_π=1nF. $\beta = 100$

Solution

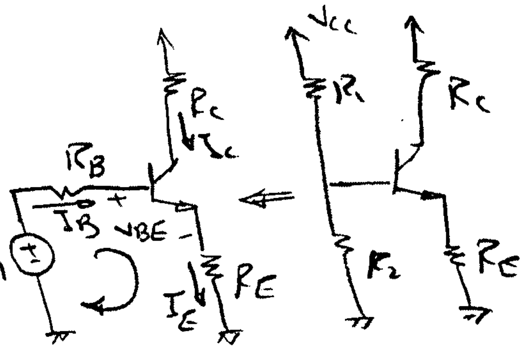


DC Analysis

- All capacitor are o.c

$R_B = R_{Th} = R_1 \| R_2 = 10K \| 10K = 5K\Omega$.

$V_{Th} = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{15 * 10}{10+10} = 7.5\ V$



Loop (I)

$V_{Th} = I_B R_B + V_{BE} + I_E R_E$; $I_B = \frac{I_E}{1+\beta}$

$I_E = \frac{V_{Th} - V_{BE}}{R_E + \frac{R_B}{1+\beta}} = \frac{7.5 - 0.7}{6.8K + \frac{5K}{101}} = 0.993\ mA$

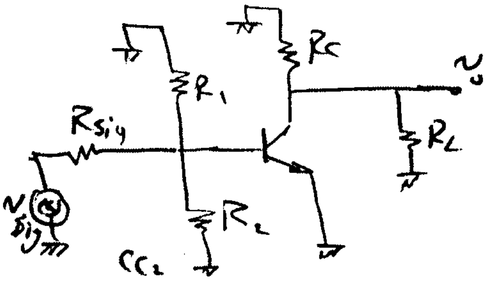
$I_C = \alpha I_E = \frac{\beta}{1+\beta} I_E = \frac{100}{101} * 0.993m = 0.98\ mA$

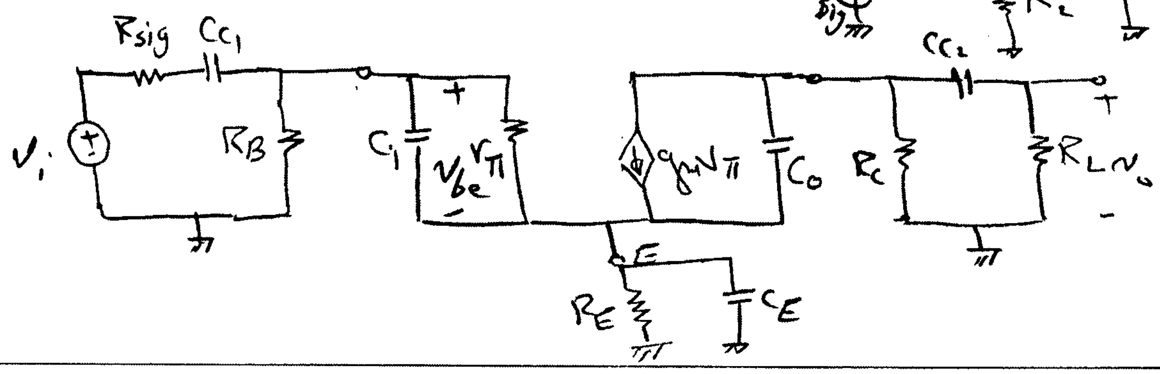
$g_m = \frac{I_C}{V_T} = \frac{0.98m}{25\ mV} = 39.2\ mA/V$

$r_\pi = \frac{\beta}{g_m} = \frac{100}{39.2m} = 2.55\ K\Omega$.

$r_o = \infty = o.c$

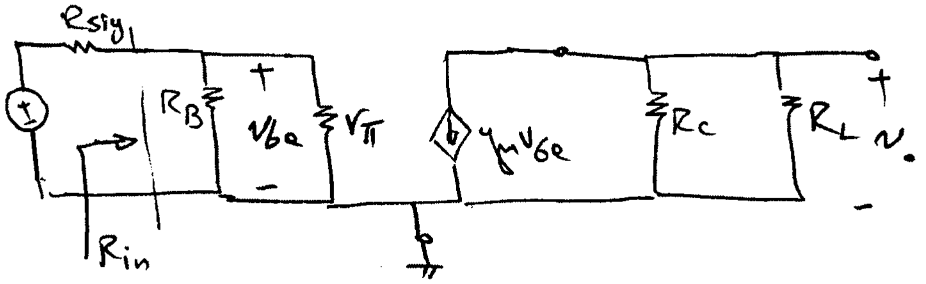
AC Analysis





For mid-band gain A_{vo} There is no effect of capacitors,

$C_{C1} = C_{C2} = C_E = S.C$ & $C_i = C_o = O.C$



$R_{in} = R_B \parallel r_\pi = 5K \parallel 2.55K = 1.69\ K\Omega$

$\left|\frac{V_{ce}}{V_{be}}\right| = g_m R_L' \quad ; \quad R_L' = R_c \parallel R_L$

$R_L' = R_c \parallel R_L = 4.3K \parallel 1K\Omega = 811.32\ \Omega$

$\left|\frac{V_{ce}}{V_{be}}\right| = 39.2 \times 10^{-3} * 811.32 = 31.8\ V/V$

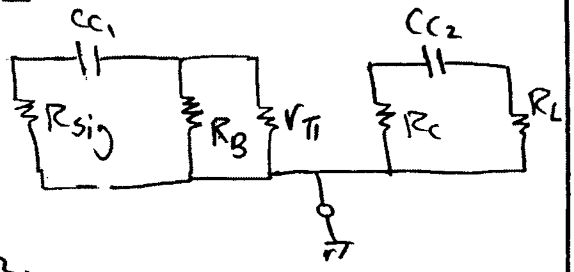
$C_i = C_\pi + C_{Mi} \quad ; \quad C_{Mi} = C_\mu\left(1 + \left|\frac{V_{ce}}{V_{be}}\right|\right)$

$C_{Mi} = 1pf(1 + 31.8) = 32.8\ pf$

$C_{Mo} = C_\mu\left(1 + \frac{1}{\left|\frac{V_{ce}}{V_{be}}\right|}\right) = C_\mu = 1\ pf = C_o$

- To find cutoff frequency ⇒ V.S = S.C & C.S = O.C
- for low frequency ⇒ $C_i = C_o = O.C$

<u>effect of C_{C1}</u>



put $C_{C2} = C_E = S.C$

$R_{CC1} = R_{sig} + R_B \parallel r_\pi$

$= 500 + 1.69K = 2.19\ K\Omega.$

$f_{CL1}\big|_{CC1} = \frac{1}{2\pi\,(C_{C1} R_{C1})} = \frac{1}{2\pi(0.47 * 10^{-6} * 2.19 \times 10^3)}$

$= 154.6\ HZ$

<u>effect of C_{C2}</u>

put $C_{C1} = C_E = S.C$

$R_{CC2} = R_C + R_L = 4.3K + 1K = 5.3\ K\Omega$

$$f_{cL_2}\Big|_{C_{C_2}} = \frac{1}{2\pi(C_{C_2} R_{C_{C_2}})}$$

$$= \frac{1}{2\pi * 0.68*10^{-6} * 5.3*10^{3}} = 44.2\ HZ$$

effect of C_E

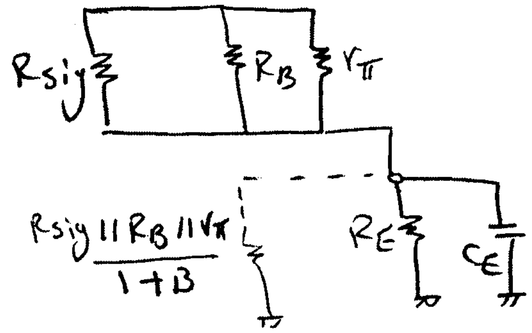
put $C_{C_1} = C_{C_2} = S.C$

$$R_{C_E} = R_E \parallel \left[\frac{R_{sig} \parallel R_B \parallel r_\pi}{1+B}\right]$$

$$= 6.8K \parallel \left[\frac{500 \parallel 1.69K}{1+B}\right]$$

$$= 6.8K \parallel \frac{385.85}{101}$$

$$= 6.8K \parallel 3.82 \simeq 3.82\ \Omega.$$



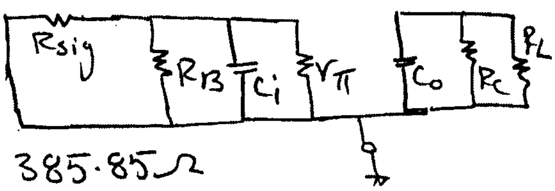
$$f_{cL_3}\Big|_{C_E} = \frac{1}{2\pi(C_E R_{C_E})} = \frac{1}{2\pi * 0.22*10^{-6} * 3.82} = 189.4\ KHZ$$

$f_L = f_{cL_1} + f_{cL_2} + f_{cL_3} = 189.6\ KHZ$

– for high frequency Response $\Rightarrow C_{C_1} = C_{C_2} = C_E = S.C$

effect of C_i

put $C_o = o.c$



$R_{C_i} = R_{sig} \parallel R_B \parallel r_\pi = 500 \parallel 1.69K = 385.85\ \Omega$

$$f_{ch_1}\Big|_{C_i} = \frac{1}{2\pi(C_i R_{C_i})}$$

$C_i = C_\pi + C_{Mi} = 1nF + 32.8\ pf = 1.0328\ nF$

$$f_{ch_1}\Big|_{C_i} = \frac{1}{2\pi * 1.0328*10^{-9} * 385.85} = 399.4\ KHZ$$

effect of C_o put $C_i = o.c$

$R_{C_o} = R_C \parallel R_L = R_L' = 811.32\ \Omega$

$$f_{ch_2}\Big|_{C_o} = \frac{1}{2\pi(C_o R_{C_o})} = \frac{1}{2\pi * 1 * 10^{-12} * 811.32} = 196.17\ MHZ$$

$f_h = f_{ch_1} + f_{ch_2} = 196.569\ MHZ$

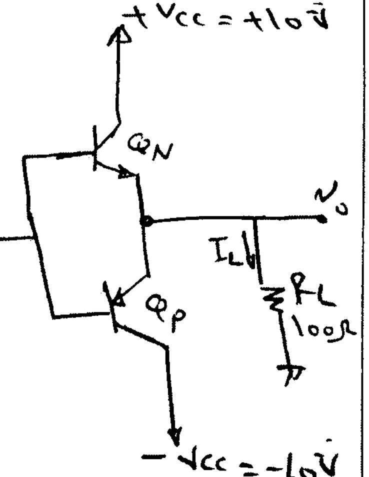
Q4:

Consider the complementary BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat}. For ±10V power supplies and a 100Ω load resistance,

a) What is the maximum sine wave output power available?

b) What is the power-conversion efficiency?

c) Show how to reduce the zero-crossing distortion in class B power amplifier?



Solution

(a) The average load power $P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$

where $\hat{V}_o$ is The peak amplitude of o/p sine wave

- The maximum sine-wave o/p power occurs when $\hat{V}_o = V_{cc}$ Then

$$P_L\Big|_{max} = \frac{1}{2}\frac{V_{cc}^2}{R_L}$$

$$= \frac{1}{2}\frac{(10)^2}{100} = 0.5\ W$$

(b) The power Conversion efficiency $\eta = \frac{P_L}{P_S}$

where P_S is The Total supply power

$$P_S = P_{S+} + P_{S-}$$

∵ The average power drawn from each of The Two Power supplies will be The same :- Then

$$P_{S+} = P_{S-} = \frac{1}{\pi}\frac{\hat{V}_o}{R_L}V_{cc} = \frac{1}{\pi}\frac{(10)}{100}\times 10 = 0.318\ W$$

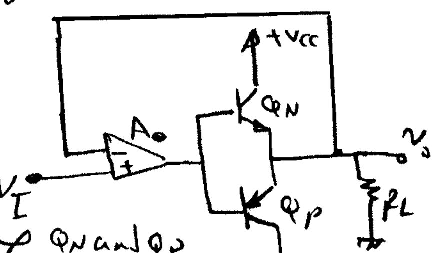
$$\therefore P_S = 2 * 0.318 = 0.637\ W$$

∴ The power Conversion efficiency η is

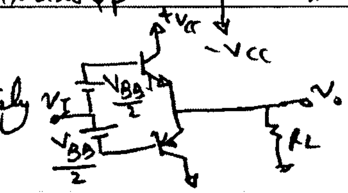
$$\eta = \frac{P_L}{P_S}\times 100 = \frac{0.5}{0.637}*100 = 78.5\ \%$$

(c) - To reduce The Zero-Crossing distortion in class B Power Amp. by using a high-gain op-Amp. and overall negative feedback as shown The ±0.7V dead band is reduced To ±0.7/A. Volt.

where A_o is The DC gain of op-Amp.

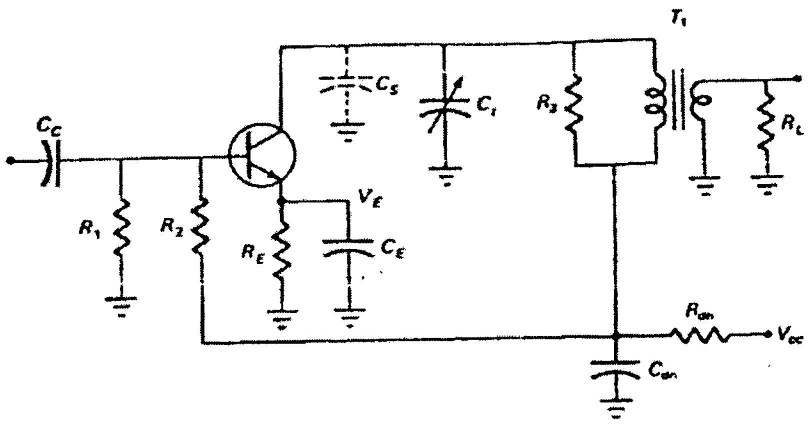


- OR by biasing The Complementary Transistors using bias voltage V_{BB} applied between The bases of QN and Qp giving rise To a bias current I_Q. Thus for small V_I, both Transistors conduct and crossover distortion is almost completely eliminated. as shown in fig. (class AB o/p stage)



Q5:

Design an RF amplifier for P_o (max) = 9 mW into R_L = 100 Ω at $w_o = 10^7$ rad/s and bandwidth of 10^6 rad/s. T_1 consists of X_{L1} = 100 Ω with Q_u = 100 at w_o and k = 1. The transistor has V_{be} = 0.7, β= 100, C_{bc} = 3 pF, and C_{be} = 27 pF. For V_{CC}=10v determine:



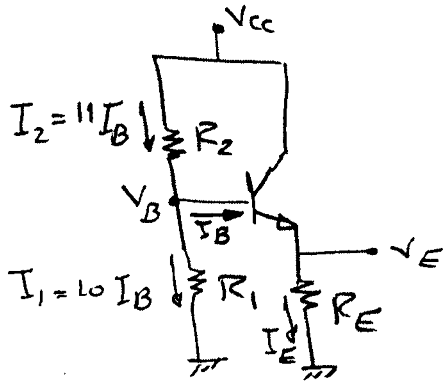
a) R_1, R_2, and R_E.

b) C_t and Turns ratio of T_1, given the bandwidth requirement.

c) Amplifier ac input resistance, R_{in}, and parallel capacitive reactance, X_{in}.

Solution

DC Design



let $\eta = 50\%$; ∵ $P_o|_{max} = 9mW$

$I_c = \frac{2P_o}{0.9V_{cc}}$

$= \frac{2*9m}{0.9*10} = 2mA$

$I_B = \frac{I_c}{\beta} = \frac{2m}{100} = 0.02mA$

$I_E = I_B + I_c = 2m + 0.02m = 2.02mA$

let $V_E = 0.1 V_{cc} = 0.1 * 10 = 1V$

$R_E = \frac{V_E}{I_E} = \frac{1}{2.02m} = 495\,\Omega$

for hard potential divider let $I_1 = 10 I_B$; Then $I_2 = 11 I_B$

∵ $V_B = V_{BE} + V_E = 0.7 + 1 = 1.7V$

∴ $R_1 = \frac{V_B}{I_1} = \frac{1.7}{10*0.02m} = 8.5K\Omega$

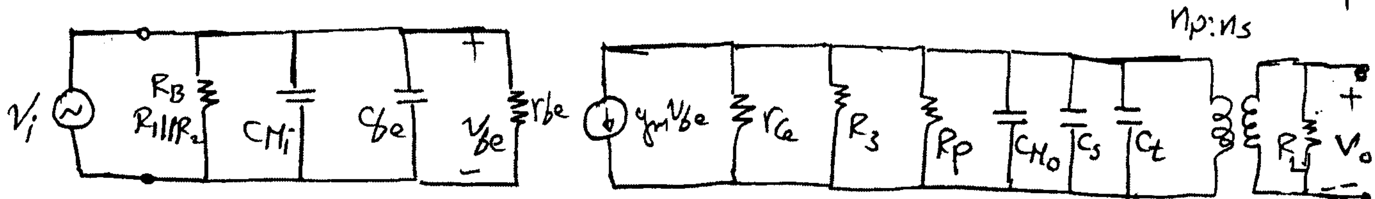
$R_2 = \frac{V_{cc} - V_B}{I_2}$

$= \frac{10 - 1.7}{11*0.02m} = 37.73K\Omega$

AC Design

$$g_m = \frac{I_c}{V_T} = \frac{2\,mA}{25\,mV} = 0.08\ A/V$$

$$r_{be} = \frac{\beta}{g_m} = \frac{100}{0.08} = 1.25\ K\Omega$$



$$Q_L = \frac{f_o}{BW} = \frac{10^7/2\pi}{10^6/2\pi} = 10$$

$$\because Q_L = \frac{R_{eq}}{\omega_o L} = \frac{R_{eq}}{X_L} \Rightarrow R_{eq} = Q_L X_L$$

$$\therefore R_{eq} = 10 * 100 = 1\ K\Omega$$

for max. power Transfer $\Rightarrow R_L' = r_{ce}'$

$$\because R_{eq} = 1K\Omega \Rightarrow R_L' = r_{ce}' = 2K\Omega$$

$$\because R_L' = R_L\left(\frac{n_p}{n_s}\right)^2 \Rightarrow \frac{n_p}{n_s} = \sqrt{\frac{R_L'}{R_L}} = \sqrt{\frac{2K}{100}} = 4.47 \cong 5$$

$$r_{ce}' = r_{ce} \parallel R_3 \parallel R_p$$

$$R_p = \omega_o L Q_u = X_L Q_u = 100 * 100 = 10\ K\Omega.$$

$$\because f_o = \frac{1}{2\pi\sqrt{L_p C_{eq}}} \Rightarrow C_{eq} = \frac{1}{(2\pi f_o)^2 L_p}$$

$$\because X_L = \omega_o L_p \Rightarrow L_p = \frac{X_L}{\omega_o} = \frac{100}{10^7} = 10\ \mu H$$

$$C_{eq} = \frac{1}{\left(2\pi \times \frac{10^7}{2\pi}\right)^2 * 10 * 10^{-6}} = 1000\ pf$$

$$\because C_{eq} = C_s + C_t + C_{Mo}$$

$C_{Mo} \cong C_{bc}$; $C_s = 0$ (not given)

$$\therefore C_t = C_{eq} - C_{Mo} = 1000\,pf - 3\,pf = 997\ pf$$

$$R_i = R_1 \parallel R_2 \parallel r_{be} = R_B \parallel r_{be} = 8.5K \parallel 37.73K \parallel 1.25K = 1.059\ K\Omega.$$

$C_{in} = C_{Mi} \parallel C_{be} = C_{Mi} + C_{be}$

$C_{Mi} = (1 + |A_{vo}|) C_{bc}$

$|A_{vo}| = \left|\frac{V_{ce}}{V_{be}}\right| = g_m R_{eq} = 0.08 * 1K\Omega = 80 \ V/V$

$C_{Mi} = (1+80) * 3pf = 243 \ pf$

$\therefore C_{in} = C_{Mi} + C_{be}$

$= 243 \ pf + 27 \ pf = 270 \ pf$

$X_{C_{in}} = \frac{1}{w_o C_{in}}$

$= \frac{1}{10^7 * 270 * 10^{-12}} = 370 \ \Omega.$