Benha university
Faculty of Engineering
Electrical Eng. Dept.
Dr Hossam Labib Zayed

Microelectronics (E301)
Final-Term Exam (corrective)
Date: 3/1/2016
Time: 3 Hours

Answer the following questions:

Q1: (a) Describe the output voltage of the circuit shown in Fig.(1). Assuming the diodes to be actual and $V_I = 10 \sin wt$. Sketch one cycle of the output voltage.

(b) Fig.(2) shows a simpler way to draw a transistor circuit. What are collector-emitter voltage and the transistor power dissipation?

Q2: The zener diode in the circuit of figure (3) has a constant reverse breakdown voltage V_Z= 8.2V, for 75mA$\leq I_Z \leq$ 1A, if $R_L = 9\ \Omega$, size R_S so that $V_L = V_Z$ is regulated to (maintained at) 8.2V while Vs varies by ±10 % percent from its nominal value of 12V.

Q3: (a) Assuming that the diodes in the circuit of Fig.(4) are ideal, find the values of the labeled voltage, V, and current, I.

(b) What is the output voltage in Fig.(5). Let β of the two transistors are very high.

Q4: The transistor in the circuit shown in fig.(6) is biased to operate in the active mode. Assuming that β is very large, find the collector bias current I_c. Replace the transistor with small-signal equivalent circuit T -model, find the values of the voltage gains of (V_{o1}/v_i) and (V_{o2}/v_i).

Q5: For the amplifier shown in Fig.(7), let V_{CC} = 12V, R_1= 22 kΩ, R_2= 6.8 kΩ, R_E = 560 Ω, and R_C = 1 kΩ. The transistor has β = 100. Calculate the dc bias current I_E. If the amplifier operates between a source for which R_{sig} = 600 Ω and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, R_o, and the voltage gain v_o/v_{sig}.

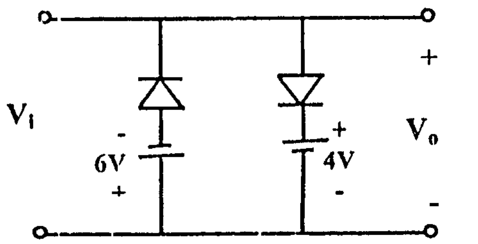


Fig. (1)

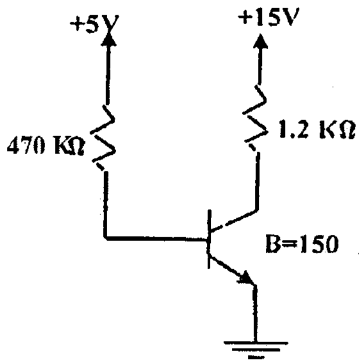


Fig.(2)

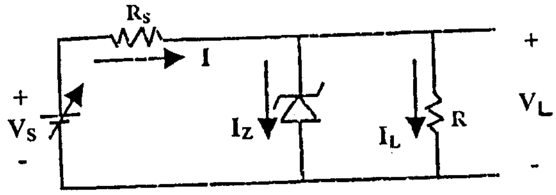


Fig.(3)

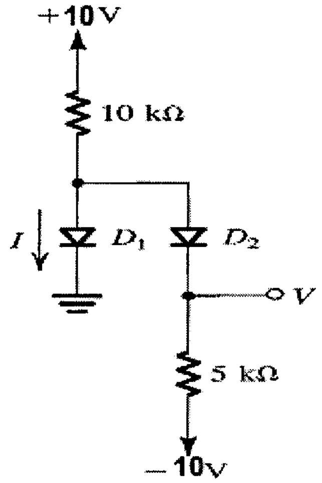


Fig.(4)

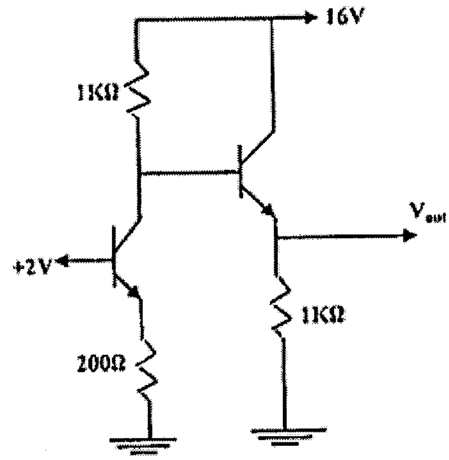


Fig.(5)

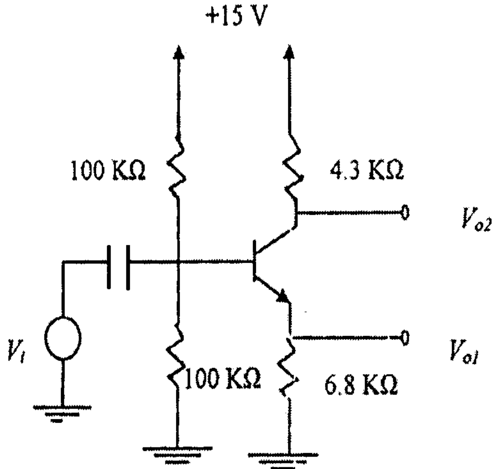


Fig.(6)

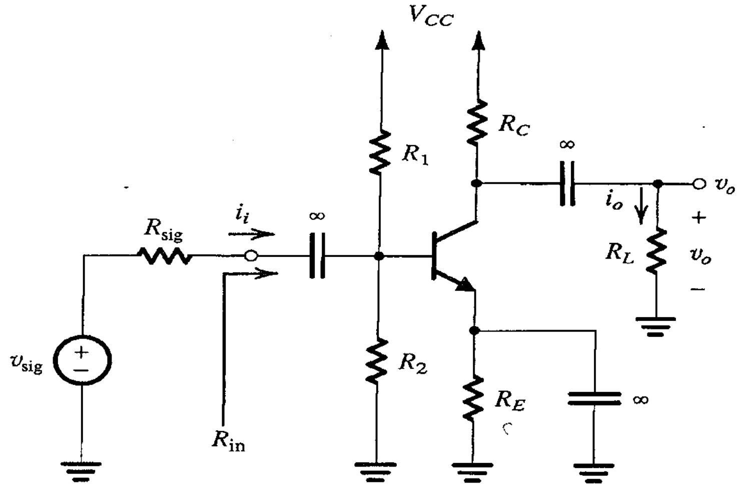


Fig.(7)

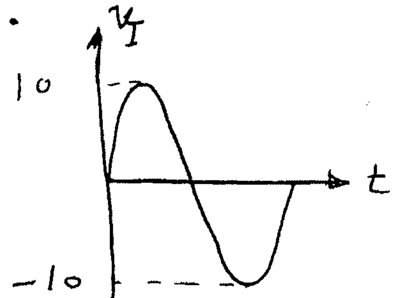
BEST WISHES

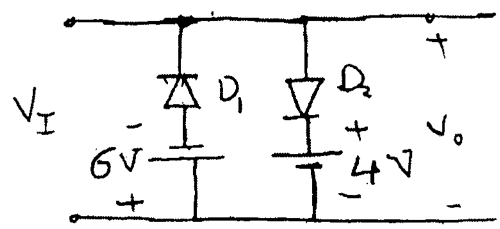
Hossam Labib

Q1 (a) (6 points)

Describe the o/p voltage of the circuit shown. Assuming the diode to be actual and $v_I = 10 \sin wt$. sketch one cycle of the o/p.

Solution .





for +ve half cycle

- for $v_i < 4.7$ V

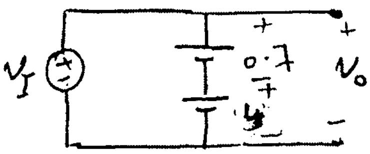
  D_1 and D_2 are off

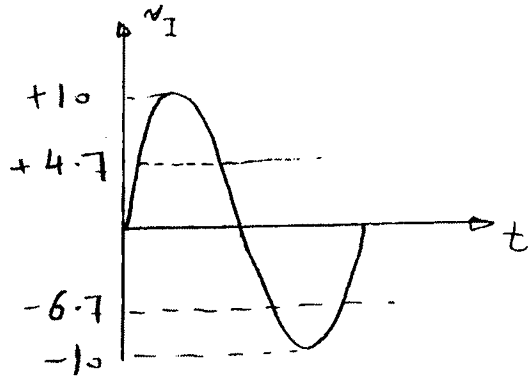
  $\therefore v_o = v_i$

- for $v_i > 4.7$ (2)

  D_1 off & D_2 on

  $\therefore V_o = 4.7$ V





for −ve half cycle

- for $v_i > -6.7$

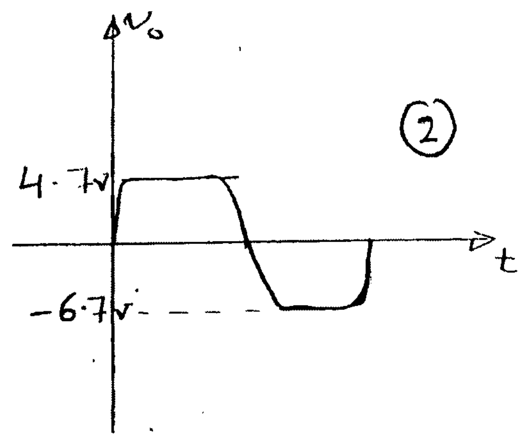
  D_1 off and D_2 off

  $\therefore v_o = v_i$ (2)

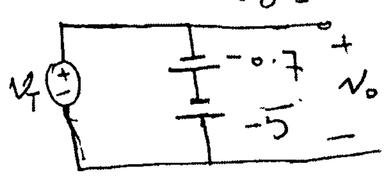
- for $v_i < -6.7$

  D_1 on & D_2 off

  $\therefore v_o = -6.7$

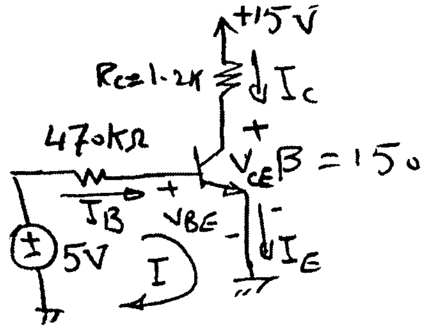


(2)



Q1 (b) (points)

Fig.(2) shows a simpler way to draw a transistor circuit. what are collector emitter voltage and the transistor power dissipation?



Solution

Let Transistor in Active Region

Loop (I)

$$5 = 470K\, I_B + V_{BE}$$

$$I_B = \frac{5 - 0.7}{470K} = 9.15\ \mu A$$

$\because I_C = \beta I_B = 150 * 9.15\mu = 1.3725\ mA$

$V_{CE} = V_{CC} - I_C R_C = 15 - 1.3725 * 1.2 = 13.353\ V$

$\because V_E = 0\ V$, $\because V_{BE} = V_B - V_E$

$\therefore V_B = V_{BE} = 0.7\ V$; $V_C = V_{CE} = 13.353\ V$

$\because V_B > V_E \Rightarrow$ BEJ Forward bias

$\because V_B < V_C \Rightarrow$ BCJ Revirse bias

$\therefore$ Transistor in Active Region

$\therefore V_{CE} = 13.353\ V$; $I_C = 1.3725\ mA$

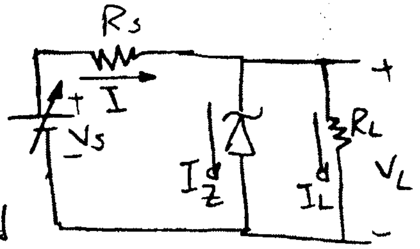
$P_{diss} = I_{CQ} V_{CEQ}$

$= 1.3725 * 10^{-3} * 13.353 = 0.0183\ w$

$= 18.3\ mw$

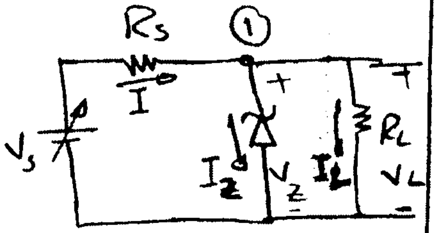
Q2: (1 points)

The Zener diode shown has a constant reverse breakdown voltage $V_Z = 8.2$ V for $75\,mA \le I_Z \le 1\,A$. If $R_L = 9\,\Omega$, size R_s so that $V_L = V_Z$ is regulated to (maintained at) 8.2 V while V_s varies by ± 10 % percent from its nominal value of 12 V



Solution

at node ①



$$I = I_Z + I_L \longrightarrow ①$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{8.2}{9} = 0.911\ A$$

$$\therefore R_s = \frac{V_s - V_Z}{I} = \frac{V_s - V_Z}{I_Z + I_L} \longrightarrow ②$$

We use ② to size R_s for max. Zener current I_Z at the largest value of V_s ; ∵ $75\,mA \le I_Z \le 1\,mA$

i.e $I_Z = 1\,A$; $V_s = V_s + 10\%\ V_s = 1.1\,V_s$
$= 1.1 * 12 = 13.2$ V

$$\therefore R_s = \frac{13.2 - 8.2}{1 + 0.911} = 2.62\ \Omega$$

- We check to see if $I_Z > 75$ mA at the lowest value of V_s i.e $V_s = V_s - 10\%\ V_s = 0.9\,V_s = 0.9 \times 12 = 10.8$ V.

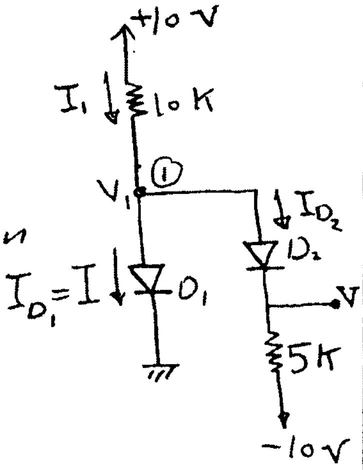
$$I_Z = I - I_L = \frac{V_s - V_Z}{R_s} - I_L = \frac{10.8 - 8.2}{2.62} - 0.911$$
$$= 0.9924 - 0.911 = \underline{81.4\ mA} > 75\ mA$$

since $I_Z > 75$ mA ; $V_Z = 8.2$ V then regulation is occured (preserved)

Q3(a)

Assuming that the diodes in the circuit of Fig.(2) are ideal, Find the values of the labeled voltage, V, and current, I.

Solution



let $I = I_{D_1}$

let D_1 and D_2 are on

For D_1 on $\Rightarrow V_1 = 0 \Rightarrow V = 0$ for D_2 on

$$\therefore I_1 = \frac{10 - V_1}{10K} = \frac{10-0}{10K} = 1mA$$

$$I_{D_2} = \frac{V_1 - (-10)}{5K} = \frac{0+10}{5K} = 2mA$$

From node ① $\Rightarrow I_1 = I_{D_1} + I_{D_2}$

$$I_{D_1} = I_1 - I_{D_2} = 1mA - 2mA = -1mA$$

$\because I_{D_1}$ -ve $\therefore$ not True

i.e the assumption not correct

Let D_1 off and D_2 on

- For D_1 off $\Rightarrow I_{D_1} = 0$; $I_1 = I_{D_2}$

- For D_2 on $\Rightarrow I_1 = \frac{10-(-10)}{10K + 5K} = \frac{20}{15K} = 1.333\ mA$

$V = I_{D_2} * 5K - 10 = 1.333 * 5 - 10 = -3.335\ V$

For $V = -3.335\ V$; $\because V_1 = V = V_{P_1} = -3.335$; $V_{n_1} = 0$

i.e $V_{P_1} < V_{n_1} \Rightarrow D_1$ off

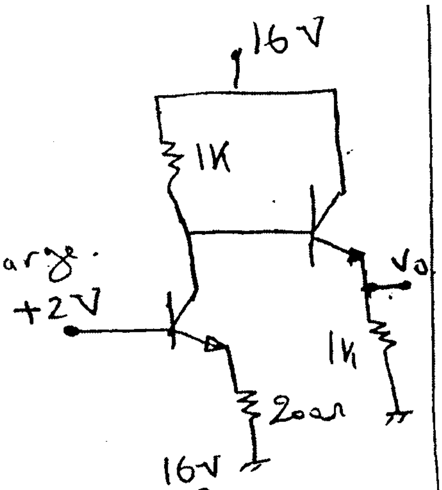
$\therefore$ The assumption is True (D_1 off & D_2 on)

$\therefore V = -3.335\ V$ and $I = I_{D_1} = 0\ A$

Q3(b): (points)

what is the o/p voltage.

- Let β of the 2-transistors is very large.

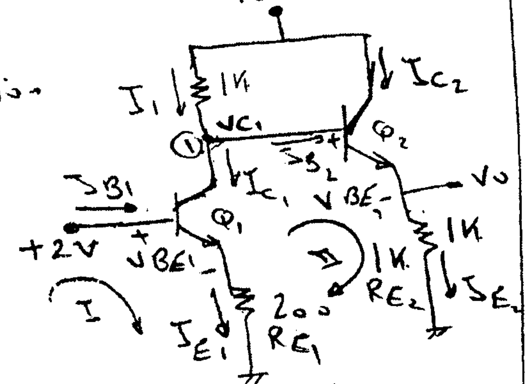


Solution

∵ β is very high

∴ $I_{B1} = I_{B2} \simeq 0$

let Q_1 and Q_2 in Active region



Loop (I)

$-2 + V_{BE1} + I_{E1} R_{E1} = 0$

$I_{E1} = \frac{2 - 0.7}{200} = 6.5 \text{ mA}$

∴ $I_{C1} = I_{E1}$

∴ at node ① ⇒ $I_1 = I_{C1} + I_{B2}$; $I_{B2} = 0$

∴ $I_1 = I_{C1} = 6.5 \text{ mA}$

$V_{C1} = 16 - I_1 * 1K = 16 - 6.5 * 1 = 9.5 \text{ V} = V_{B2}$

$V_{E1} = I_{E1} R_{E1} = 6.5 * 0.2 = 1.3 \text{ V}$

Loop (II)

$-V_{C1} + V_{BE2} + I_{E2} R_{E2} = 0$

$I_{E2} = \frac{9.5 - 0.7}{1K} = 8.8 \text{ mA}$

∴ $V_o = I_{E2} R_{E2} = 8.8 * 1 = 8.8 \text{ V} = V_{E2}$

$V_{C2} = 16 \text{ V}$

for Q_1 ∵ $V_{B1} > V_{E1}$ ⇒ BEJ → Forward

$V_{B1} < V_{C1}$ ⇒ BCJ → Reverse

∴ Q_1 in Active region

for Q_2 ∵ $V_{B2} > V_{E2}$ ⇒ BEJ → Forward.

$V_{B2} < V_{C2}$ ⇒ BCJ → Reverse

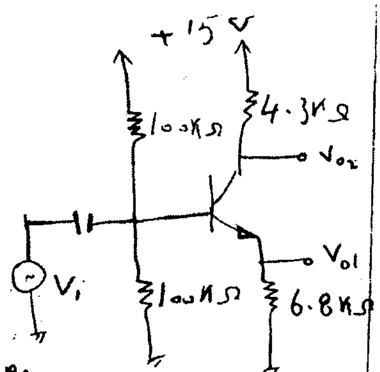
∴ Q_2 in Active region.

∴ Assumption is True.

∴ $V_o = V_{E2} = 8.8 \text{ V}$

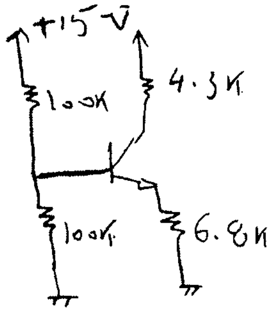
Q4: (points)

The Transistor in the circuit shown is biased to operate in the active mode. Assuming That β is very Large, find The collector bias current. Replace the Transistor with small-signal equivalent circuit T-Model, find the values of the voltage gains of V_{o1}, V_{o2}.



Solution

DC analysis

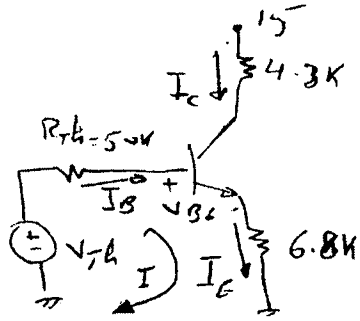


reduce AC sources i.e V_i = s.c

and ALL capacitor are o.c

$$V_{Th} = 15 \frac{100K}{100K + 100K} = 7.5 \text{ V}$$

$$R_{Th} = 100K \,//\, 100K = 50 K\Omega.$$



∴ β is very Large $\Rightarrow I_B = 0$

, $\alpha = 1$ & $I_C = I_E$

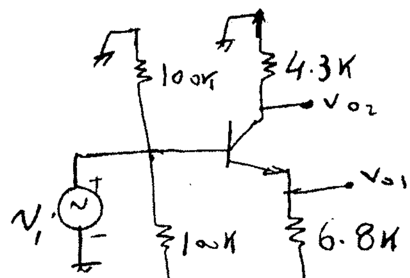
Loop (I)

$$-V_{Th} + I_B R_{Th} + V_{BE} + 6.8K\, I_E = 0$$

$$I_E = \frac{V_{Th} - V_{BE}}{6.8K} = \frac{7.5 - 0.7}{6.8K} = 1 mA$$

∴ $I_C = 1 mA$

Ac analysis



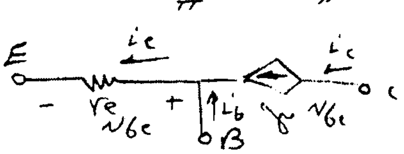
reduce DC sources V_{CC} = s.c

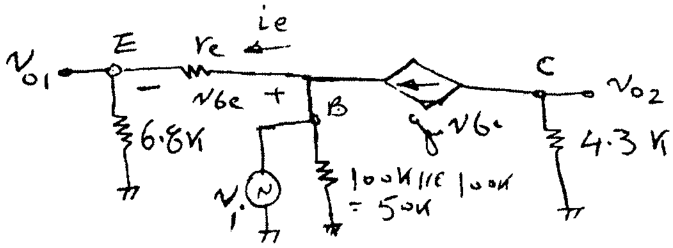
ALL capacitor are s.c

The parameters of T-Model are

$$g_m = \frac{I_C}{V_T} = \frac{1 mA}{25 mV} = 40 mA/V$$

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m} = 25 \Omega.$$





$$v_{o2} = -g_m v_{be} \times 4.3K$$

$$v_{be} = v_i \frac{r_e}{r_e + 6.8K}$$

$$v_{o2} = -g_m v_i \frac{r_e * 4.3K}{r_e + 6.8K}$$

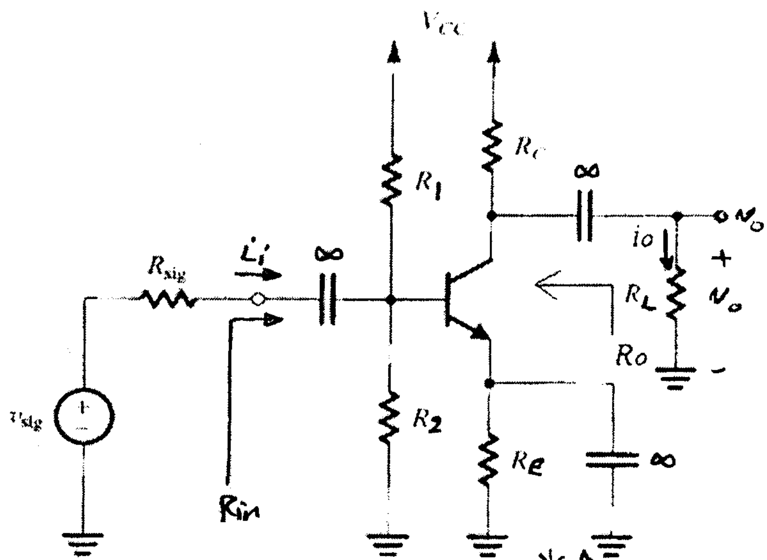
$$\frac{v_{o2}}{v_i} = -g_m \frac{r_e \times 4.3K}{r_e + 6.8K} = -40 \times 10^{-3} \frac{25 \times 4300}{25 + 6800} = -0.63\ V/V$$

$$\# \quad v_{o1} = v_i \frac{6.8K}{6.8K + r_e}$$

$$\frac{v_{o1}}{v_i} = \frac{6.8K}{6.8K + 25} = 0.996\ V/V$$

(Q5)

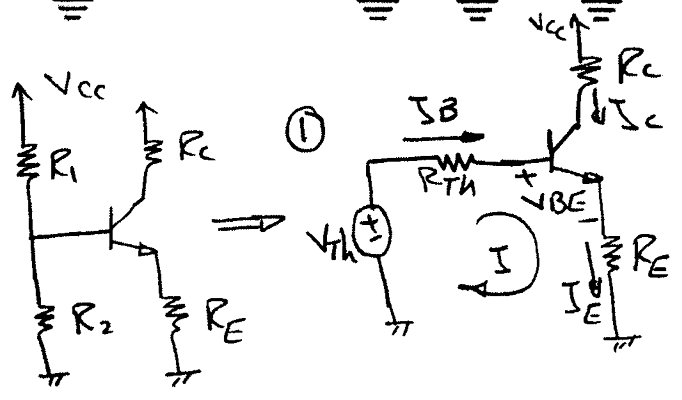
For the amplifier shown in Fig.(3), let V_{CC} = 12V, R_1 = 22 kΩ, R_2 = 6.8 kΩ, R_E = 560 Ω, and R_C = 1 kΩ. The transistor has β = 100. Calculate the dc bias current I_E. If the amplifier operates between a source for which R_{sig} = 600 Ω and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, R_o, and the voltage gain v_o/v_{sig}.



Solution

DC Analysis

- ALL capacitor are o-c
- Reduce AC sources



$R_{Th} = R_1 \parallel R_2 = 22K \parallel 6.8K$

$R_{Th} = 5.19 \, K\Omega$

$V_{Th} = V_{cc} \dfrac{R_2}{R_1 + R_2}$

$V_{Th} = 12 \dfrac{6.8K}{22K + 6.8K} = 2.833 \, V$

Loop (I)

$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$; $\because I_E = (1+\beta) I_B$

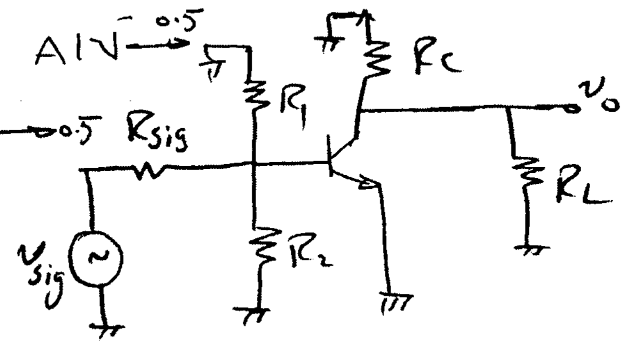
$\dfrac{I_E}{1+\beta} R_{Th} + I_E R_E = V_{Th} - V_{BE}$

$I_E = \dfrac{V_{Th} - V_{BE}}{R_E + \dfrac{R_{Th}}{1+\beta}} = \dfrac{2.833 - 0.7}{560 + \dfrac{5.19K}{101}} = 3.489 \, mA \longrightarrow ①$

$I_C = \alpha I_E = \dfrac{\beta}{1+\beta} I_E = \dfrac{100}{101} * 3.489 \, mA = 3.454 \, mA$

$g_m = \dfrac{I_C}{V_T} = \dfrac{3.454 \, mA}{25 \, mV} = 0.138 \, A/V \xrightarrow{0.5}$

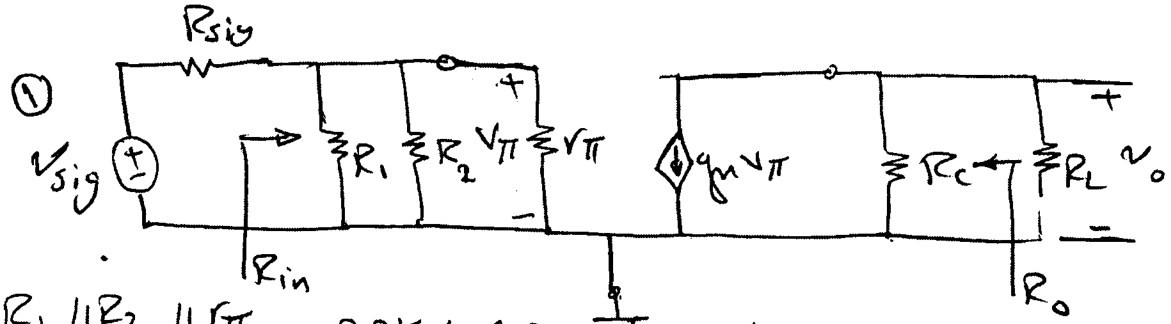
$r_\pi = \dfrac{\beta}{g_m} = \dfrac{100}{0.138} = 724.64 \, \Omega \longrightarrow 0.5$



- AC Analysis

- ALL capacitor are s.c
- reduce DC sources

using π-model



$R_{in} = R_1 \| R_2 \| r_\pi = 22K \| 6.8K \| 724.61$

$= 635.93 \simeq 636\,\Omega$ ⟶ ①

$R_o |_{v_{sig}=0} = R_C = 1\,K\Omega.$ ⟶ ①

To find $\frac{v_o}{v_{sig}}$:-

$v_o = -g_m v_\pi (R_C \| R_L)$

$v_\pi = v_{sig} \frac{R_{in}}{R_{in} + R_{sig}}$

$v_o = -g_m v_{sig} \frac{R_{in}}{R_{in}+R_{sig}} (R_C \| R_L)$ ⟶ ②

$\frac{v_o}{v_{sig}} = -g_m \frac{R_{in}}{R_{in}+R_{sig}} (R_C \| R_L)$

$= -0.138 \frac{636}{636 + 600} (1K \| 2K)$

$= -0.138 * 0.515 * 666.667 = -47.34$ V/V ⟶ ①