Faculty of Engineering
Benha university
Electrical Eng.Dept.
Dr Hossam Labib Zayed

Microelectronics (E302)
Final-Term Exam (June 2013)
Data: 21/5/2013
Time: 3 Hours

Answer the following questions:

Q1: Complete the following sentences:

i. The family of FET transistors may be divided into: ….. and …… .
ii. The …….. MOSFET has a physical channel between the drain and source.
iii. The high input resistance of a JFET is due to ………….. .
iv. The non-inverting configuration has a gain greater than or equally................
v. The....... detectors can be used to produce a square wave from a sine wave.
vi. The feedback element in an integrator is ……….
vii. The bandwidth of the ideal op amp is approximately equal to …….
viii. The input stage of every op amp is ……….amplifier.
ix. When same signals are applied to the inputs of a differential amplifier it known as….. .
x. The input differential resistance of BJT differential amplifier is equal to ……
xi. ………… is a measure of a differential amplifier’s ability to reject common mode signal.

Q2: (a) the NMOS transistors in the circuit of Fig. (1) have $V_t = 1V$, $\mu_n C_{ox} = 120\ \mu A/V^2$, $\lambda = 0$, and $L_1 = L_2 = L3 = 1\mu m$. Find the required values of gate width for each of Q_1, Q_2, and Q_3 to obtain the voltages and current values indicated.

(b) Find the input resistance of the circuit shown in Fig.(2). Assuming ideal op amp, $R_1 = 10\ k\Omega$, $R_2 = 100\ k\Omega$, and $R_3 = 5\ k\Omega$.

Q3: A common gate amplifier using an n-channel E-MOS transistor for which g_m=5mA/V, shown in Fig.(3), has R_D=5KΩ, and R_L=2 KΩ. The amplifier is driven by voltage source having a 200Ω resistance. What are the input resistance and the overall voltage gain of the amplifier? If the circuits allow a bias current increase by a factor of 4 while maintaining linear operation, what do the input resistance and voltage gain become?

Q4: The two op amps in the circuit shown in fig.(4) are ideal. Find v_o ,i_x and i_o.

Q5: Find the overall voltage gain v_o/v_s and the differential input resistance of the amplifier shown in fig. (5). Assuming β = 100.

PTO

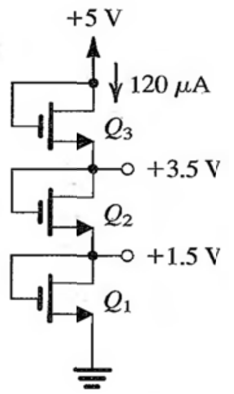

Fig.(1)

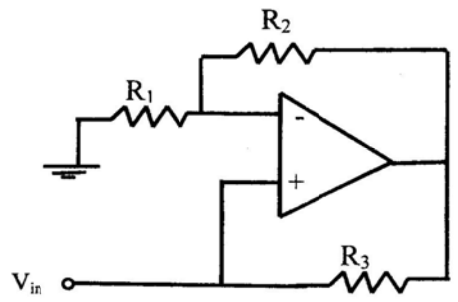

Fig.(2)

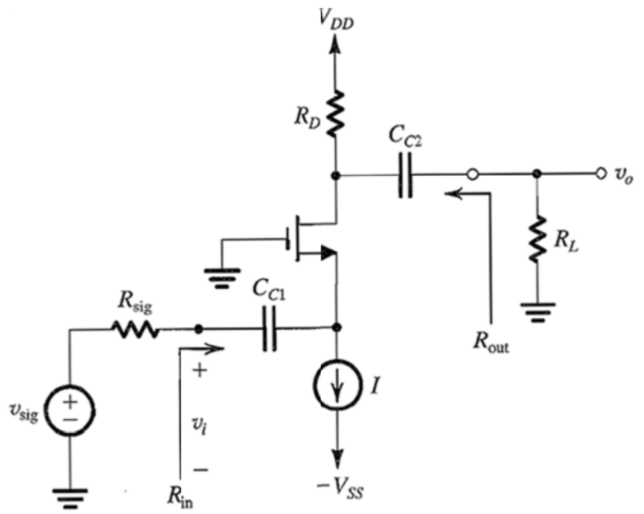

Fig.(3)

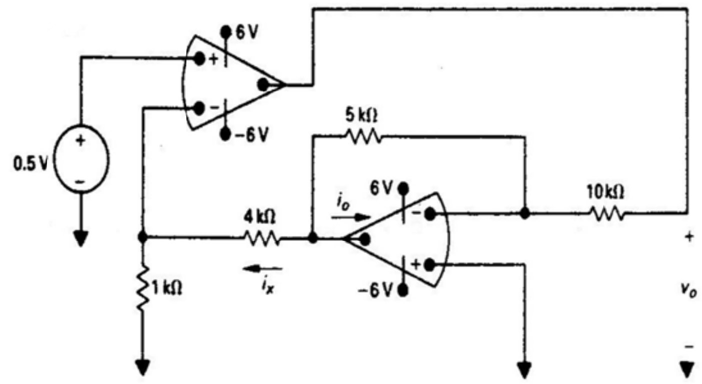

Fig.(4)

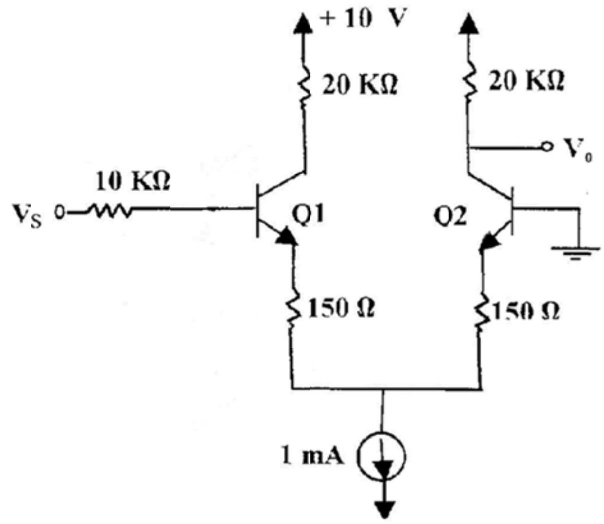

Fig.(5)

BEST WISHES

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Model Answer

Q1: Complete the following sentences:

i. The family of FET transistors may be divided into: Junction FET (JFET) and Metal-Oxide-Semiconductor FET (MOSFET)

ii. The depletion MOSFET has a physical channel between the drain and source.

iii. The high input resistance of a JFET is due to the reverse-biased gate source junction.

iv. The non-inverting configuration has a gain greater than or equally one.

v. The zero crossing detectors can be used to produce a square wave from a sine wave.

vi. The feedback element in an integrator is a capacitor.

vii. The bandwidth of the ideal op amp is approximately equal to ∞.

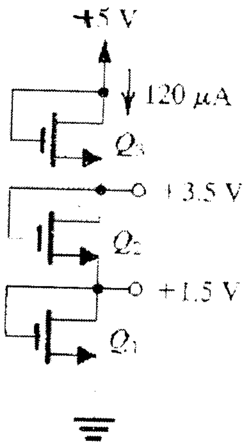
viii. The input stage of every op amp is a differential amplifier.

ix. When same signals are applied to the inputs of a differential amplifier it known as common mode signal.

x. The input differential resistance of BJT differential amplifier is equal to $(1+\beta)2r_e$.

xi. CMRR is a measure of a differential amplifier's ability to reject common mode signal.

Q2: (a) the NMOS transistors in the circuit of Fig. (1) have $V_t = 1V$, $\mu_n C_{ox} = 120\ \mu A/V^2$, $\lambda = 0$, and $L_1 = L_2 = L3 = 1\mu m$. Find the required values of gate width for each of Q_1,Q_2, and Q_3 to obtain the voltages and current values indicated.



Solution

$I_{D1} = I_{D2} = I_{D3} = 120\ \mu A$

for Q_1

$V_{S1} = 0$ & $V_{G1} = V_{D1} = 1.5\ V$

$V_{GS1} = V_{G1} - V_{S1} = 1.5\ V$

$V_{DS1} = V_{D1} - V_{S1} = 1.5\ V$

$V_{DS1}|_{sat} = V_{GS1} - V_t = 1.5 - 1 = 0.5\ V$

$\because V_{DS1} > V_{DS}|_{sat}$ $\therefore Q_1$ in Saturation Region

$I_{D1} = K_1 (V_{GS1} - V_t)^2$

$$K_1 = \frac{I_{D1}}{(V_{GS1} - V_t)^2} = \frac{120\ \mu A}{(0.5)^2} = 480\ \mu A/V^2$$

$$\because K_1 = \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} \Rightarrow W_1 = \frac{2 K_1 L_1}{\mu_n C_{ox}}$$

$$W_1 = \frac{2 * 480 \times 10^{-6} * 1 * 10^{-6}}{120 * 10^{-6}} = 8\ \mu m$$

for Q_2

$V_{S2} = 1.5\ V$; $V_{G2} = V_{D2} = 3.5\ V$

$V_{GS2} = V_{G2} - V_{S2} = 3.5 - 1.5 = 2\ V$

$V_{DS2} = V_{D2} - V_{S2} = 3.5 - 1.5 = 2\ V$

$V_{DS2}|_{sat} = V_{GS2} - V_t = 2 - 1 = 1\ V$

$V_{DS2} > V_{DS2}|_{sat} \Rightarrow Q_2$ in Saturation Region

$$K_2 = \frac{I_{D2}}{(V_{GS2} - V_t)^2} = \frac{120\ \mu A}{(1)^2} = 120\ \mu A/V^2$$

$$W_2 = \frac{2 K_2 L_2}{\mu_n C_{ox}} = \frac{2 * 120 \times 10^{-6} \times 10^{-6}}{120 \times 10^{-6}} = 2\ \mu m$$

for Q_3 $V_{S3} = 3.5\ V$; $V_{G3} = V_{D3} = 5\ V$

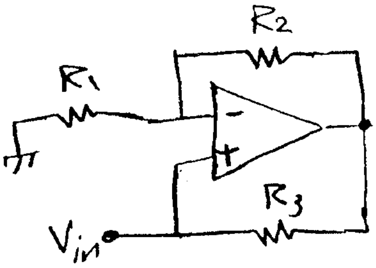
$V_{GS3} = V_{G3} - V_{S3} = 5 - 3.5 = 1.5\ V = V_{DS3} \Rightarrow Q_3$ in Saturation

$$K_3 = \frac{I_{D3}}{(V_{GS3} - V_t)^2} = \frac{120\ \mu A}{(0.5)^2} = 480\ \mu A/V^2$$

$\Rightarrow W_3 = W_1 = 8\ \mu m$

Q2:(b) (6 POINTS)

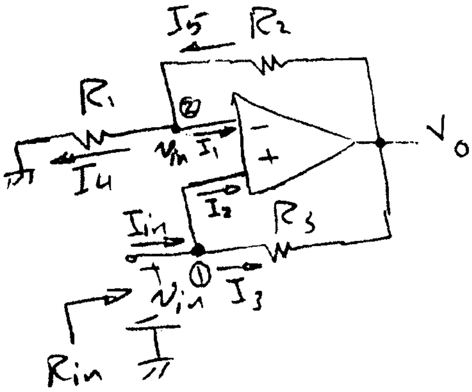
Find the input resistance Rin of the circuit shown. Assume ideal op Amp. and $R_1 = 10\ K\Omega$, $R_2 = 100\ K\Omega$, $R_3 = 5\ K\Omega$.



Solution

Apply I/P voltage and evaluate the I/P current Iin thus

$$R_{in} = \frac{V_{in}}{I_{in}}$$



at node ①

$$I_{in} = I_2 + I_3 \qquad ; \quad I_1 = I_2 = 0$$

$$I_{in} = I_3 = \frac{V_{in} - V_o}{R_3} \longrightarrow ① \quad ; \quad V^+ = V^- = V_{in}$$

at node ②

$$I_5 = I_4 + I_1 \qquad ; \quad I_1 = 0$$

$$I_5 = I_4 \Longrightarrow \frac{V_1 - 0}{R_1} = \frac{V_o - V^-}{R_2}$$

$$\frac{V_{in}}{R_1} = \frac{V_o - V_{in}}{R_2} \Longrightarrow V_{in}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{V_o}{R_2}$$

$$V_o = V_{in}\left(1 + \frac{R_2}{R_1}\right) \longrightarrow ②$$

from ① $\Longrightarrow$ $$I_{in} = \frac{V_{in}}{R_3} - \frac{V_o}{R_3} = \frac{V_{in}}{R_3} - \frac{V_{in}}{R_3}\left(1 + \frac{R_2}{R_1}\right)$$

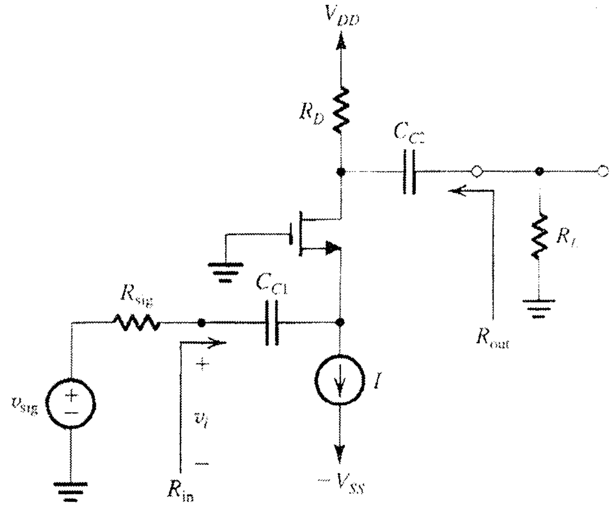
$$I_{in} = \frac{V_{in}}{R_3}\left(1 - 1 - \frac{R_2}{R_1}\right) = \frac{V_{in}}{R_3}\left(-\frac{R_2}{R_1}\right)$$

$$\therefore R_{in} = \frac{V_{in}}{I_{in}} = -R_3\left(\frac{R_1}{R_2}\right)$$

[this circuit is called negative Impedance converter (NIC)]

$$R_{in} = -\left(\frac{5K * 10K}{100K}\right) = -0.5\ K\Omega.$$

Q3: A common gate amplifier using an n-channel E-MOS transistor for which g_m=5mA/V, shown in Fig., has R_D=5KΩ, and R_L=2 KΩ. The amplifier is driven by voltage source having a 200Ω resistance. What are the input resistance and the overall voltage gain of the amplifier? If the circuits allow a bias current increase by a factor of 4 while maintaining linear operation, what do the input resistance and voltage gain become?

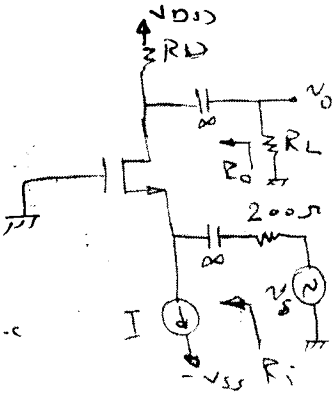


Solution:

$g_m = 5$ mA/V

$R_L = 2$ KΩ & $R_D = 5$ KΩ

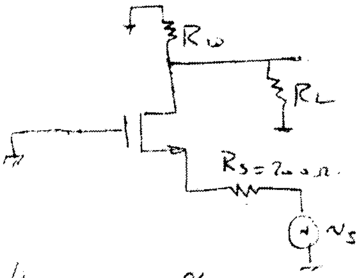
$R_S = 200$ Ω

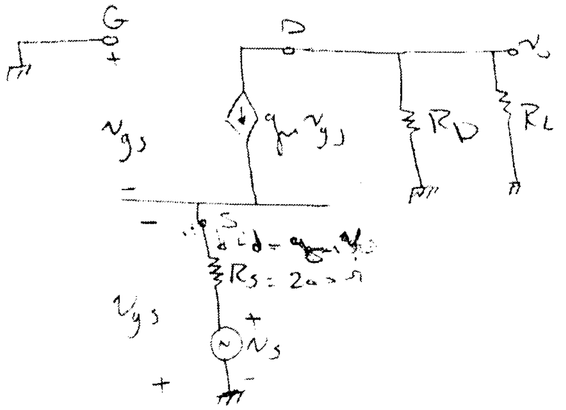


AC analysis

All capacitors S.C

reduce dc sources i.e V.S = S.C & C.S = O.C





To find $A_v = \frac{v_o}{v_s}$

$$v_o = -g_m v_{gs}(R_D \parallel R_L)$$

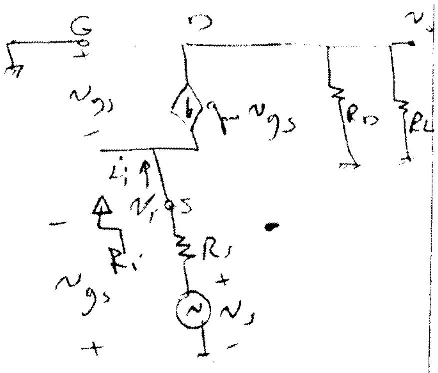
$$-v_{gs} = g_m v_{gs} R_s + v_s$$

$$v_{gs}(1 + g_m R_s) = -v_s$$

$$v_{gs} = \frac{-v_s}{1 + g_m R_s}$$

$$v_o = +g_m \frac{v_s}{1 + g_m R_s}(R_D \parallel R_L)$$

$$\frac{v_o}{v_s} = \frac{g_m}{1 + g_m R_s}(R_D \parallel R_L) = \frac{5\times10^{-3}}{1 + 200 \times 5\times10^{-3}}(2K \parallel 5K) = 3.57$$



$R_i = \frac{v_i}{i_i}$

$i_i = -g_m v_{gs}$

$v_i = -v_{gs}$

$\therefore R_i = \frac{-v_{gs}}{-g_m v_{gs}} = \frac{1}{g_m}$

$= \frac{1}{5 \times 10^{-3}} = 200\ \Omega$

(b)

$\because g_m = 2\sqrt{K I_D}$

$g_{m1} = 2\sqrt{K I_{D1}}$; $g_{m1} = 5\ mA/V$

If I_D increase by factor 4 $\Rightarrow I_{D2} = 4 I_{D1}$

$\therefore g_{m2} = 2\sqrt{K I_{D2}} = 2\sqrt{K \times 4 I_{D1}} = 2(2\sqrt{K I_{D1}})$

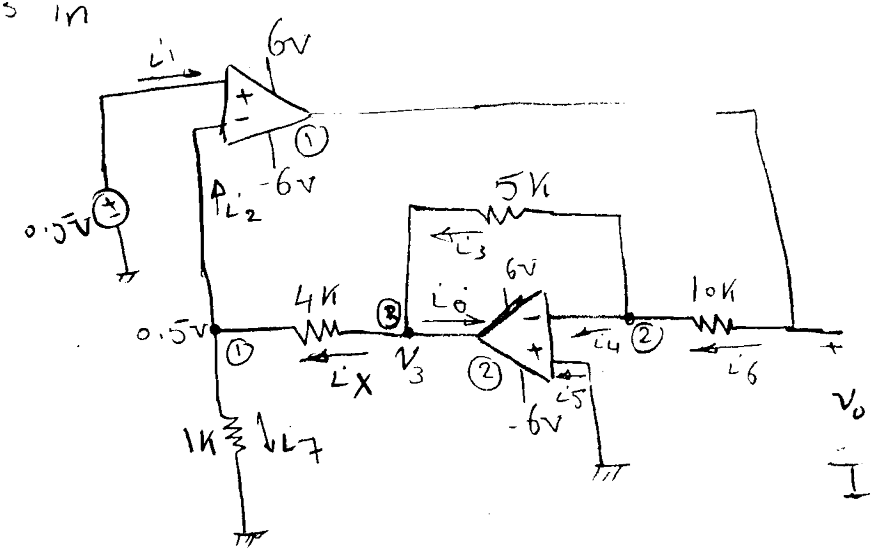
$g_{m2} = 2 g_{m1} = 2 \times 5m = 10\ mA/V$

$\therefore R_i = \frac{1}{g_{m2}} = \frac{1}{10m} = 100\ \Omega.$

$\frac{v_o}{v_s} = \frac{g_{m2}}{1 + g_{m2} R_s} (R_D \| R_L)$

$= \frac{10 \times 10^{-3}}{1 + 10 \times 10^{-3} \times 200} (2k \| 5k) = 4.76\ V/V$

Q4: The Two op Amps in the Circuit shown are ideal. Find v_o, i_x and i_o



solution

For op Amp ① $\Rightarrow v_1^+ = v_1^- = 0.5\,V$

$i_1 = i_2 = 0$

at node ①

$i_2 + i_7 = i_x \qquad ; i_2 = 0$

$i_x = i_7 \Rightarrow i_x = \frac{0.5}{1K} = 0.5\,mA$

For op Amp ② $\Rightarrow v_2^+ = v_2^- = 0 \qquad ; i_4 = i_5 = 0$

at node ②

$i_6 = i_3 + i_4 \qquad ; i_4 = 0$

$i_6 = i_3 \Rightarrow \frac{v_o - v_2^-}{10K} = \frac{v_2^- - v_3}{5K} \Rightarrow \frac{v_o}{10K} = \frac{-v_3}{5K} \quad * 5K$

$0.5\, v_o = -v_3 \Rightarrow v_o = -2\, v_3 \longrightarrow$ [1]

$\because v_3 = i_x * 4K + 0.5V = 0.5m \times 4K + 0.5 = 2.5\,V$

$v_o = -2 * 2.5 = -5\,V \Rightarrow v_o = -5\,V$

at node ③

$i_3 = i_o + i_x \Rightarrow i_o = i_3 - i_x$

$i_o = \frac{-v_3}{5K} - 0.5m = \frac{-2.5}{5K} - 0.5m = -0.5m - 0.5m$

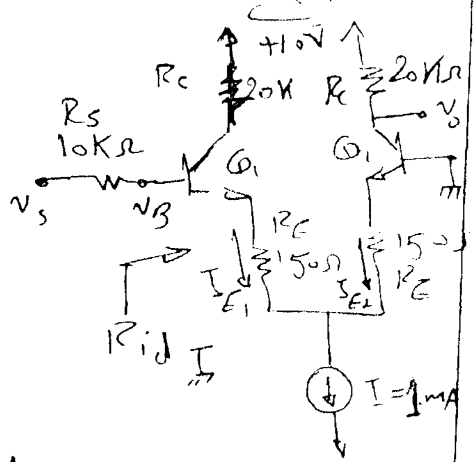
$i_o = -1\,mA$

Q5:-

Find the overall voltage gain v_o/v_s and the differential input resistance of the amplifier shown. Assuming $\beta = 100$

Solution

DC Analysis



$$I_{E_1} = I_{E_2} = I_E = \frac{I}{2}$$

$$I_E = \frac{1mA}{2} = 0.5 mA \longrightarrow 2$$

$$I_C = \alpha I_E = 0.99 I_E$$
$$= 0.99 \times 0.5m = 0.495 mA \simeq 0.5 mA$$

$$r_e = \frac{V_T}{I_E} = \frac{25 mV}{0.5 mA} = 50 \Omega \longrightarrow 1$$

$$g_m = \frac{I_C}{V_T} = \frac{0.5 mA}{25 mV} = 20 mA/V$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{20m} = 5000\Omega = 5K\Omega$$

$$R_{id} = (1+\beta)(2R_E + 2r_e) = (1+100)(2 \times 150 + 2 \times 50) = 40.4 K\Omega \longrightarrow 3$$

$$\frac{v_o}{v_s} = \frac{v_o}{v_B} \times \frac{v_B}{v_s} \longrightarrow 1$$

$$\frac{v_o}{v_B} = \frac{R_C}{2R_E + 2r_e} = \frac{20K}{2 \times 150 + 2 \times 50} = 50 \longrightarrow 2$$

$$v_B = v_s \frac{R_{id}}{R_{id} + R_s}$$

$$\frac{v_B}{v_s} = \frac{R_{id}}{R_{id} + R_s} = \frac{40.4 K}{(40.4K + 10)K} = 0.802 \longrightarrow 1$$

$$\frac{v_o}{v_s} = 0.802 \times 50 = 40.1 \longrightarrow 2$$