Faculty of Engineering
Benha university
Electrical Eng.Dept.
Dr Hossam Labib Zayed

Electronic Circuits (b) (E1204)
Final-Term Exam
Data: 5/6/2014
Time: 3 Hours

Answer the following questions:

Q1: Complete the following sentences:

i. The high input resistance of a JFET is due to..... .
ii. MOSFETs differ from JFETs in that the gate of a MOSFET is insulated from the channel by ....., whereas the gate and channel in a JFET are separated by ..... .
iii. Like JFETs, the ..... can operate with $V_{GS} = 0$ V.
iv. ..... is the constant drain current when $V_{GS} = 0$.
v. The maximum voltage gain is.....in the common drain amplifier.
vi. The..... detectors can be used to produce a square wave from a sine wave.
vii. The feedback element in an integrator is .....
viii. The bandwidth of the ideal op amp is approximately equal to .....
ix. The non-inverting configuration has a gain greater than or equally.....
x. ..... is the basis of a very-high-speed logic circuit family, called emitter-coupled logic (ECL).
xi. When opposite polarity signal are applied to the inputs of a differential amplifier it known as ..... .
xii. The input differential resistance of BJT differential amplifier with emitter resistance exists is equal to ..... .
xiii. The differential amplifier responds to a differential input signal and completely ..... a common mode signal.
xiv. A higher CMRR results in a lower ..... .

Q2: (a) The parameters of the transistor p-channel JFET in the circuit shown in Fig.(1) are: I_{DSS}=2.5mA, V_P=2.5V, and λ=0. The transistor is biased with a constant current source. Calculate I_D, V_{GS} and V_{SD}.

(b) The input signal in Fig.(2) is applied to the comparator. For R_1=22kΩ and R_2=3.3kΩ draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator are ±12V.

Q3: Consider the amplifier circuit in Figure (3) with transistor parameters V_{TN}=0.8V, $\mu_n C_{ox}$ = 0.1 mA/V^2, W/L=20, and λ=0.02V^{-1}. If I_Q=5mA using T-model determine the small-signal voltage gain, the input resistance R_{in}, and the output resistance R_o.

Q4: The two op amps in the circuit shown in Fig.(4) are ideal. Find v_o ,i_x and i_o.

Q5: The differential amplifier shown in Fig.(5) uses transistors with $\beta = 100$.

a) For $v_{B1} = v_d/2$ and $v_{B2} = -v_d/2$, where v_d is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_d|$, and R_{id}.
b) For $v_{B1} = v_{B2} = v_{CM}$, find the magnitude of the common mode gain, $|v_o/v_{CM}|$.
c) Calculate the CMRR

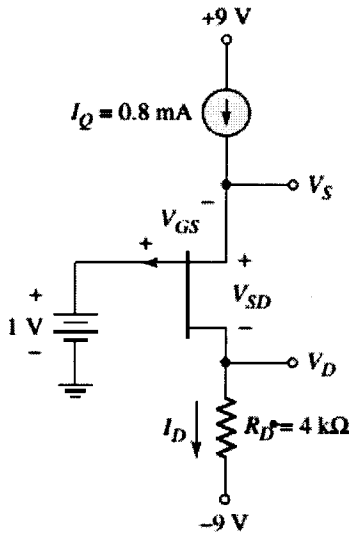
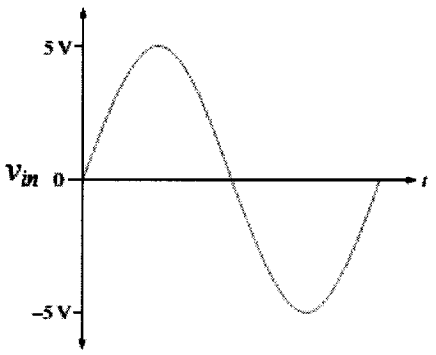


Fig.(1)



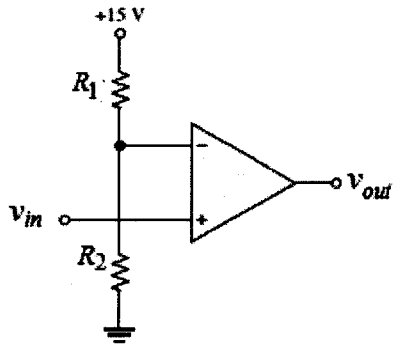


Fig.(2)

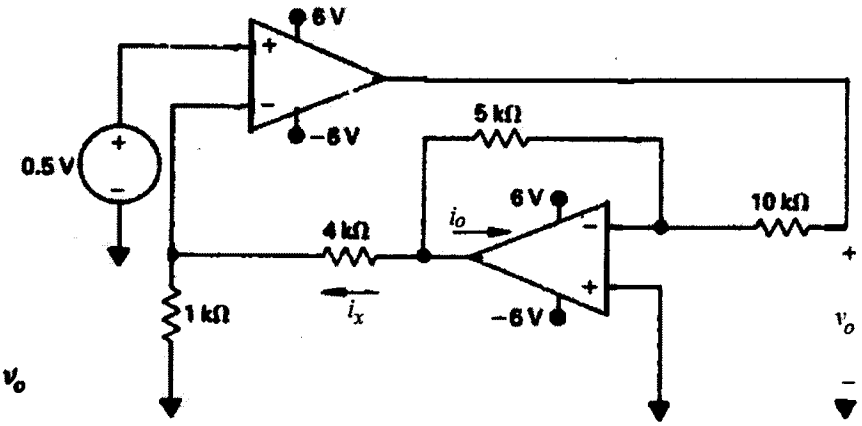


Fig.(4)

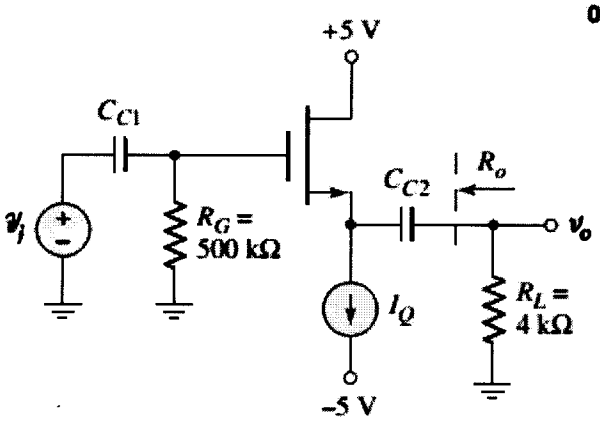


Fig.(3)

Fig.(5)

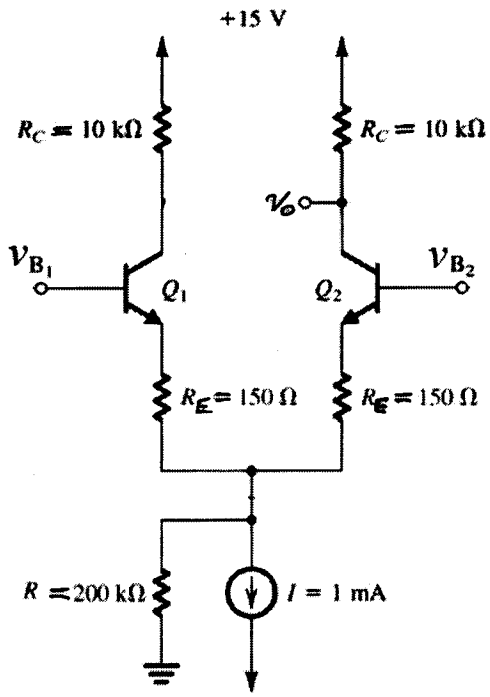


Fig.(4)

BEST WISHES

Hossam

Labib

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Answer the following questions:

Q1: Complete the following sentences:

i. The high input resistance of a JFET is due to *the reverse-biased gate-source junction.*

ii. MOSFETs differ from JFETs in that the gate of a MOSFET is insulated from the channel by *a SiO2 layer*, whereas the gate and channel in a JFET are separated by *a pn junction.*

iii. Like JFETs, the *depletion MOSFET* can operate with $V_{GS} = 0$ V.

iv. I_{DSS} is the constant drain current when $V_{GS} = 0$.

v. The maximum voltage gain is *one* in the common drain amplifier.

vi. The *zero crossing* detectors can be used to produce a square wave from a sine wave.

vii. The feedback element in an integrator is *a capacitor*.

viii. The bandwidth of the ideal op amp is approximately equal to ∞.

ix. The non-inverting configuration has a gain greater than or equally *one*.

x. *The BJT differential amplifier* is the basis of a very-high-speed logic circuit family, called emitter-coupled logic (ECL).

xi. When opposite polarity signal are applied to the inputs of a differential amplifier it known as *a differential input signal*.

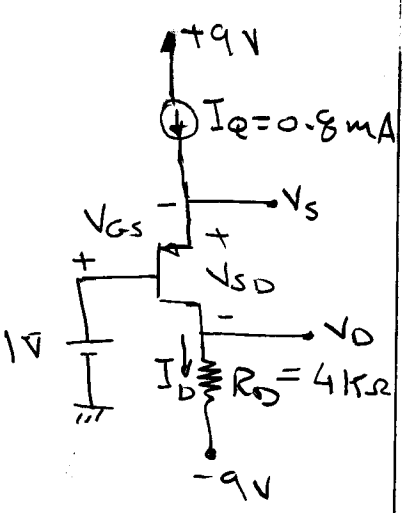
xii. The input differential resistance of BJT differential amplifier with emitter resistance exists is equal to $(1+\beta)(2r_e+2R_E)$.

xiii. The differential amplifier responds to a differential input signal and completely *rejects* a common mode signal.

xiv. A higher CMRR results in a lower *common-mode gain* A_{cm}.

Q2: (a)

The parameters of the Transistor in the circuit shown in Fig are: $I_{DSS} = 2.5\,mA$; $V_p = +2.5\,V$ and $\lambda = 0$. The Transistor is biased with a constant current source I_Q.



find I_D, V_{GS} and V_{SD}

Solution

$I_D = I_Q = 0.8\ mA$ for $I_G = 0$

$\therefore I_D = \dfrac{V_D - (-9)}{R_D} \Rightarrow V_D = I_D R_D - 9$

$V_D = 0.8m \times 4k - 9 = 3.2 - 9 = -5.8\ V$

let Transistor In saturation Region

$\therefore I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_p}\right)^2$

$0.8 = 2.5\left(1 - \dfrac{V_{GS}}{2.5}\right)^2$

$\left(1 - \dfrac{V_{GS}}{2.5}\right) = \sqrt{\dfrac{0.8}{2.5}} = \pm 0.566$

$V_{GS} = 2.5\,(1 \mp 0.566)$

$V_{GS} = 1.085\ V \lesssim V_p$ OR $V_{GS} = 3.915\ X > V_p$ (for P-channel JFET)

$\therefore V_{GS} = 1.085\ V$

$\because V_{GS} = V_G - V_S$; $V_G = 1\ V$

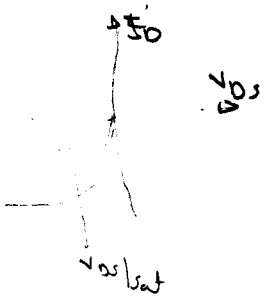
$\therefore V_S = V_G - V_{GS} = 1 - 1.085 = -0.085\ V$

$\therefore V_{SD} = V_S - V_D = -0.085 + 5.8 = 5.715\ V$

$\therefore V_{DS} = -V_{SD} = -5.715\ V$

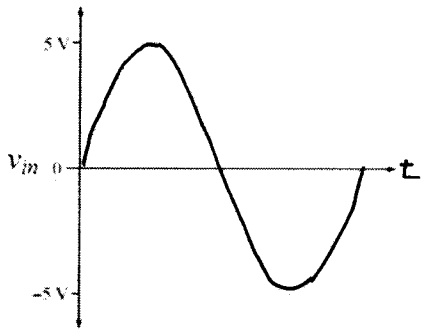
$V_{DS}|_{sat} = V_{GS} - V_p = 1.085 - 2.5 = -1.415\ V$

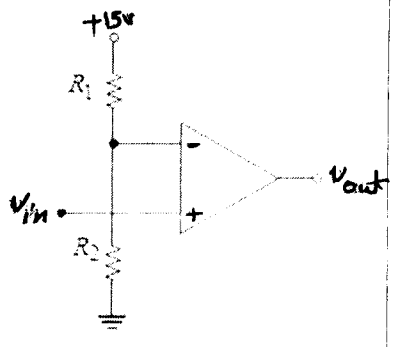
$\because V_{DS} < V_{DS}|_{sat} \Rightarrow$ Transistor is biased in saturation Region, as assumed.



Q2:(b)

The input signal in Fig.(2) is applied to the comparator. For R_1=22kΩ and R_2=3.3kΩ draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator are ±12V.



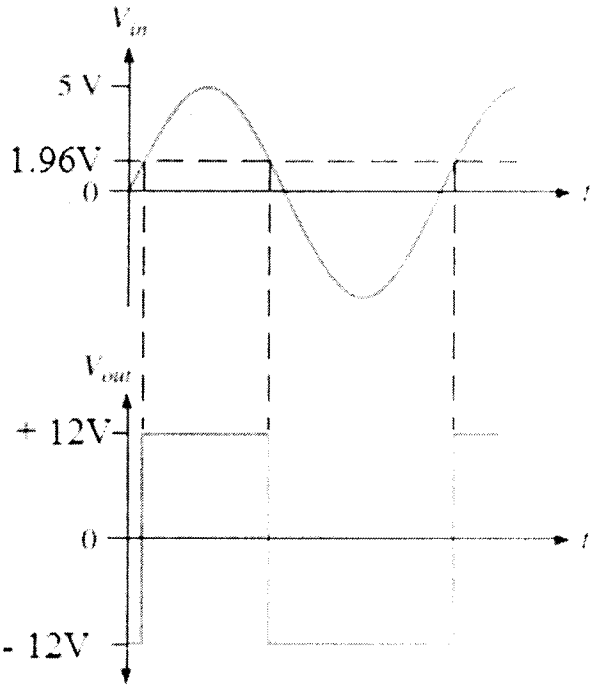


Solution:

The comparator is non zero level detector

$$V_{ref} = \frac{15 * R_2}{R_1 + R_2} =$$

$$= \frac{15 * 3.3k}{22k + 3.3k} = 1.96\,V$$



for non-Inverting comparator

- for $V_i < V_{ref}$ (1.96V)

  $\therefore V_o = -V_{sat} = -12V$

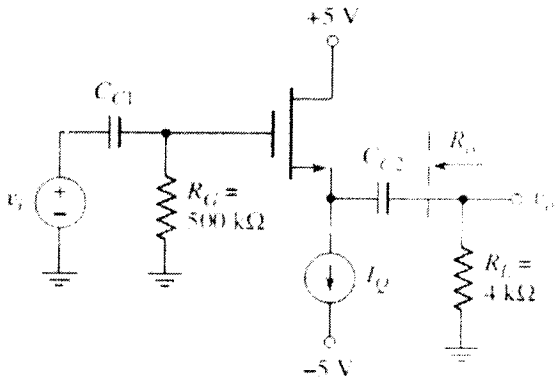
- for $V_i > V_{ref}$ (1.96V)

  $\therefore V_o = +V_{sat} = +12V$

The o/p signal is PWM

Q3:

Consider the amplifier circuit in Figure (3) with transistor parameters V_{TN}=0.8V, $\mu_n C_{ox}$ = 0.1 mA/V^2, W/L=20, and λ=0.02V^{-1}. If I_Q=5mA using T-model determine the small-signal voltage gain, the input resistance R_{in}, and the output resistance R_o



Solution

DC Analysis

$I_D = I_Q = 5mA$

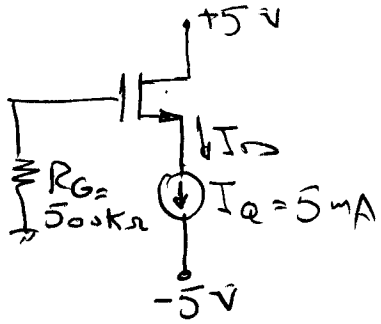
$K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = \frac{1}{2} * 0.1 * 10^{-3} * 20 = 1mA/V^2$

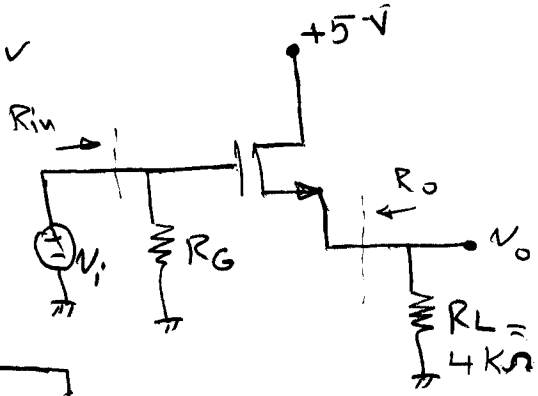
$V_A = \frac{1}{\lambda} = \frac{1}{0.02} = 50\ V$

$r_o = \frac{V_A}{I_D} = \frac{50}{5m} = 10\ K\Omega$

$g_m = 2\sqrt{K_n I_D} = 2\sqrt{1m * 5m} = 4.47\ mA/V$

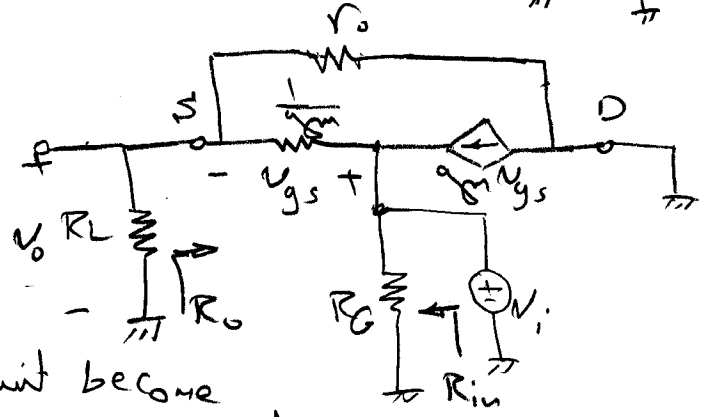
$\frac{1}{g_m} = 223.6\ \Omega$



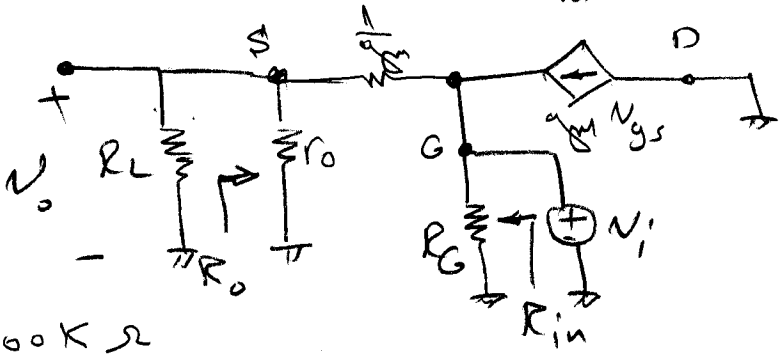


Ac Analysis

using T-model



$r_o \| R_L \Rightarrow$ The circuit become



$R_{in} = R_G = 500\ K\Omega$

Q3: Cont.

To find $A_v = \frac{V_o}{V_i}$

from voltage divider

$$V_o = \frac{V_i (R_L \| r_o)}{(R_L \| r_o) + \frac{1}{g_m}}$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

$$= \frac{(4K \| 10K)}{(4K \| 10K) + 223.6}$$

$$= \frac{2.857K}{2.857K + 223.6} = 0.927 \text{ V/V}$$

To Find R_o

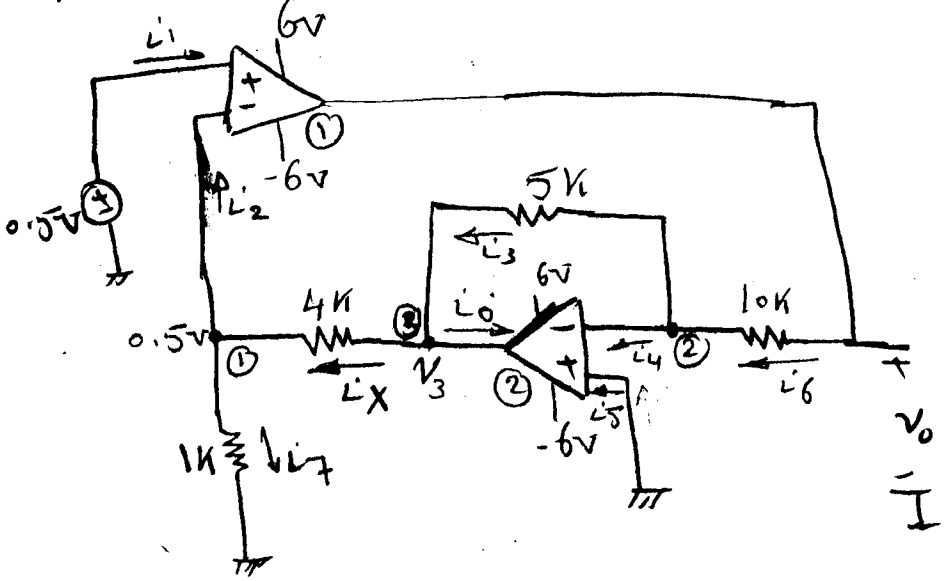
$$R_o \Big|_{V_i = 0} = r_o \| \frac{1}{g_m}$$

$$= 10K \| 223.6$$

$$= 218.71\ \Omega \simeq 219\ \Omega$$

Q4:

The Two op Amps in the circuit shown are ideal. Find v_o, i_x and i_o



Solution

For op Amp ① $\Rightarrow v_1^+ = v_1 = 0.5\,V$

$i_1 = i_2 = 0$

at node ①

$i_2 + i_7 = i_x$; $i_2 = 0$

$i_x = i_7 \Rightarrow i_x = \frac{0.5}{1K} = 0.5\ mA$

For op Amp ② $\Rightarrow v_2^+ = v_2 = 0$; $i_4 = i_5 = 0$

at node ②

$i_6 = i_3 + i_4$; $i_4 = 0$

$i_6 = i_3 \Rightarrow \frac{v_o - v_2}{10K} = \frac{v_2 - v_3}{5K} \Rightarrow \frac{v_o}{10K} = \frac{-v_3}{5K}$ *5K

$0.5\,v_o = -v_3 \Rightarrow v_o = -2v_3 \longrightarrow [1]$

$\because v_3 = i_x \times 4K + 0.5V = 0.5m \times 4K + 0.5 = 2.5\ V$

$v_o = -2 * 2.5 = -5\ V \Rightarrow v_o = -5\ V$

at node ③

$i_3 = i_o + i_x \Rightarrow i_o = i_3 - i_x$

$i_o = \frac{-v_3}{5K} - 0.5m = \frac{-2.5}{5K} - 0.5\ m = -0.5m - 0.5m$

$i_o = -1\ mA$

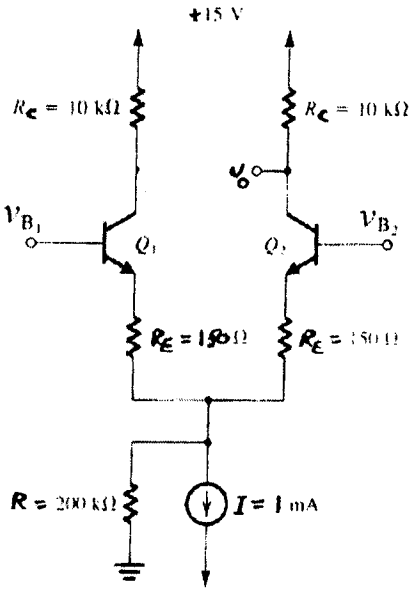
Q5:

The differential amplifier shown in fig. (5) uses transistors with $\beta = 100$.

a) For $v_{B1} = v_d/2$ and $v_{B2} = -v_d/2$, where v_d is a small signal with zero average, find the magnitude of the differential gain, (v_o/v_d), and the input differential resistance R_{id}.

b) For $v_{B1} = v_{B2} = v_{CM}$, find the magnitude of the common mode gain, (v_o/v_{CM}).

c) Calculate the CMRR.



Solution

From DC Analysis $\Rightarrow I_{E_1} = I_{E_2} = I_E = \frac{I}{2}$

$I_E = \frac{1mA}{2} = 0.5\ mA$

$r_{e_1} = r_{e_2} = r_e = \frac{V_T}{I_E} = \frac{25mV}{0.5mA} = 50\ \Omega$

$g_m = \frac{I_C}{V_T} \simeq \frac{0.5m}{25m} = 0.02\ A/V$

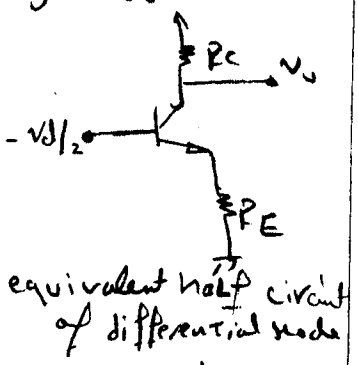
(a) For $v_{B_1} = v_d/2$ and $v_{B_2} = -v_d/2$ the o/p is Taken single ended

$|A_d|_{\text{single ended}} = \frac{R_c}{2r_e + 2R_E}$

$= \frac{10K}{2*50 + 2*150} = 25\ V/V$

$R_{id} = (1+\beta)\,2(r_e + R_E)$

$= 101 * 2 * (50+150) = 40.4\ K\Omega$

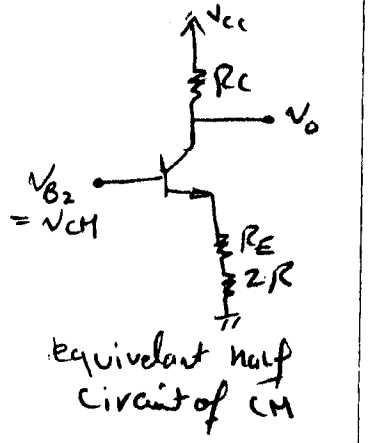


equivalent half circuit of differential mode

(b) For $v_{B_1} = v_{B_2} = v_{CM}$ $\Rightarrow$ Common Mode gain

$|A_{CM}|_{\text{single ended}} = \frac{R_c}{r_e + R_E + 2R} \simeq \frac{R_c}{2R}$; $2R \gg (r_e + R_E)$

$= \frac{10K}{50+150+2*200K} = 0.025\ V/V$



equivalent half circuit of CM

(c) $CMRR = \frac{|A_d|}{|A_{CM}|} = \frac{25}{0.025} = 1000$

$CMRR|_{dB} = 20 \log 1000 = 60\ dB$.